Every 15 msec, the μP routes *n* bytes of data from memory to the parallel-in/serial-out shift register IC_1. The 4-bit counter IC_2 causes the register to shift out this data in 8-pulse bursts. The data bytes allow the latched shift registers (IC_3, IC_4, etc) to produce the required segment and common-plane (CP) waveforms **(Fig 2).**

When the CP signal is a logic 1, all on segments are logic 0 and all off segments are logic 1. This relationship between the CP and segment signals remains in effect even though, on alternate I/O cycles, the μP complements all data bytes fetched from memory. The resident software makes necessary changes in the stored data when the display is updated.

The Clock input frequency must provide at least eight periods between successive $\overline{\text{IOSELECT}}$ pulses from the μP. Note also that the 74HC595 outputs will change while the chips are receiving serial data unless you place the outputs in a high-impedance state by driving $\overline{\text{DISPDIS}}$ high (pin 13). **EDN**

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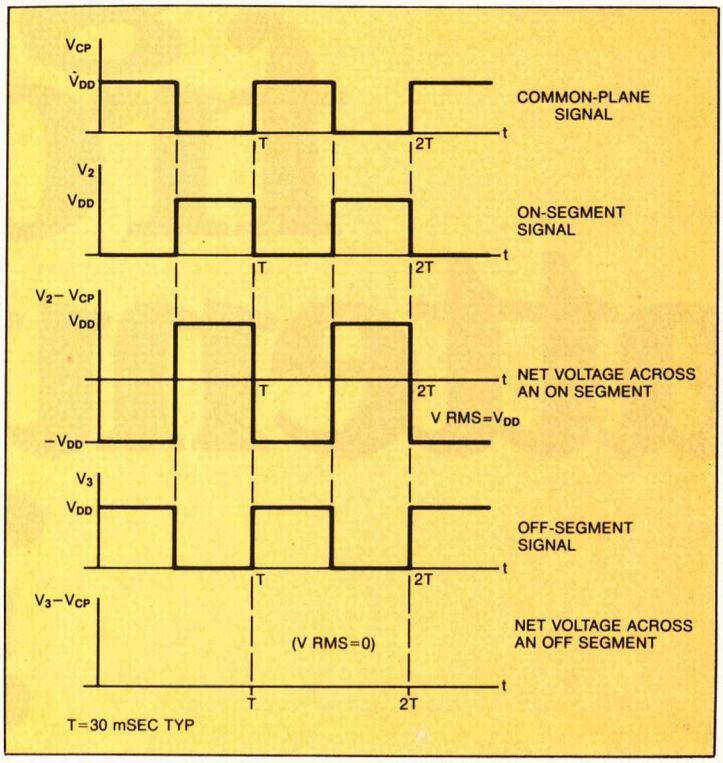

***Fig 2—These waveforms show** the polarity and time relationships for typical LCD-drive signals.*

Transistor array squares control current

Burkhard Braach
Wandel & Goltermann, Eningen, West Germany

A simple 5-transistor array and a resistor **(Fig 1)** generate a square-law relationship between I_{IN} and I_{OUT}. The circuit is useful in PLL frequency synthesizers and other closed-loop systems requiring square-law amplification in the feedback path.

Assume that the transistor base currents are negligible and that Q_1-Q_2 and Q_4-Q_5 have negligible base-emitter offset voltages. These transistor pairs then form ideal current mirrors, and their collector currents equal the input current:

$$I_1 = I_2 = I_4 = I_5 = I_{IN}. \quad (1)$$

The Q_1 and Q_3 collector currents are

$$I_1 = I_S e^{\frac{qV_{BE1}}{KT}} \text{ and } I_3 = I_S e^{\frac{qV_{BE3}}{KT}},$$

respectively, and their ratio is

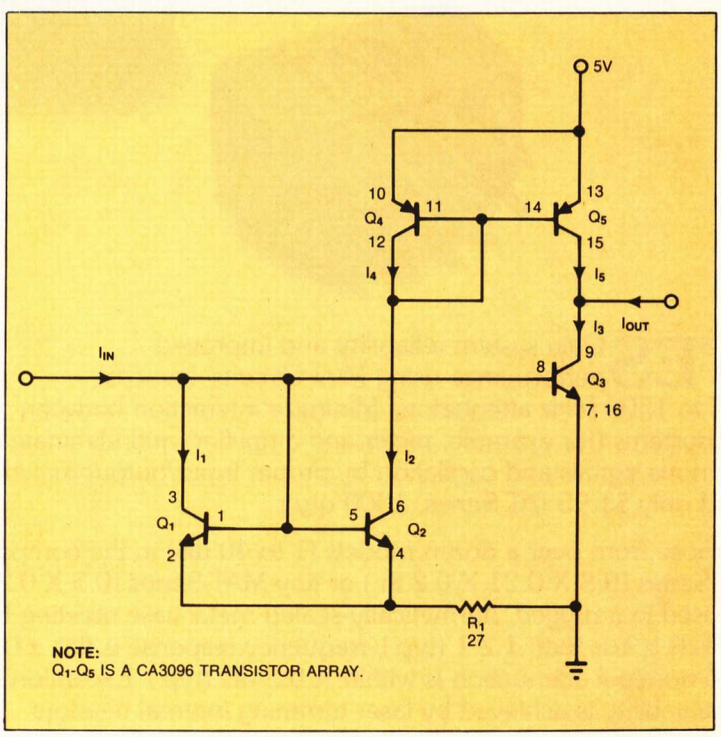

***Fig 1—This transistor-array circuit** performs square-law amplification of I_{IN}.*

$$\frac{I_3}{I_1} = e^{\frac{q(V_{BE3} - V_{BE1})}{KT}}, \quad (2)$$

where I_S=saturation current, q=electron charge, K=Boltzmann's constant, T=absolute temperature, and V_{BE1} and V_{BE3} are the base-emitter voltages for transistors Q_1 and Q_3.

Because $V_{BE3}=V_{BE1}+R_1(I_1+I_2)$, you can write **Eq 2** as

$$I_3 = I_1 e^{\frac{q(I_1 + I_2)R_1}{KT}}.$$

Substituting I_{IN} from **Eq 1** yields

$$I_3 = I_{IN} e^{\frac{2qI_{IN}R_1}{KT}}.$$

Thus, transistor Q_3 provides an exponential function that you can expand as a power series in the form of $e^x=1+x/1!+x^2/2!+x^3/3!+\ldots$ to yield

$$I_3 = I_{IN}\left[1 + \frac{2qI_{IN}R_1}{KT} + \left(\frac{2qI_{IN}R_1}{KT}\right)^2/2 + \left(\frac{2qI_{IN}R_1}{KT}\right)^3/6 + \cdots\right]. \quad (3)$$

The output current is $I_{OUT}=I_3-I_5=I_3-I_{IN}$. Substituting for I_3 (**Eq 3**) eliminates the linear term, so the series begins with the quadratic term:

$$I_{OUT} = \left(\frac{2qR_1}{KT}\right)I_{IN}^2 + \left(\frac{2qR_1}{KT}\right)^2 I_{IN}^3/2 + \left(\frac{2qR_1}{KT}\right)^3 I_{IN}^4/6 + \cdots.$$

In short, the circuit produces a useful squaring characteristic for low $2qR_1/KT$ ratios and low input currents. **Fig 2** shows the measured and calculated results for a CA3096 transistor array and a 27Ω resistor. You can extend the 20:1 output-current range by using transistor pairs with tighter V_{BE} matching and higher betas. If desired, you can reverse the output-current polarity by inserting a resistor with a value $2R_1$ in the emitter of Q_4 (remove the Q_1-Q_2 emitter resistor in this case). **EDN**

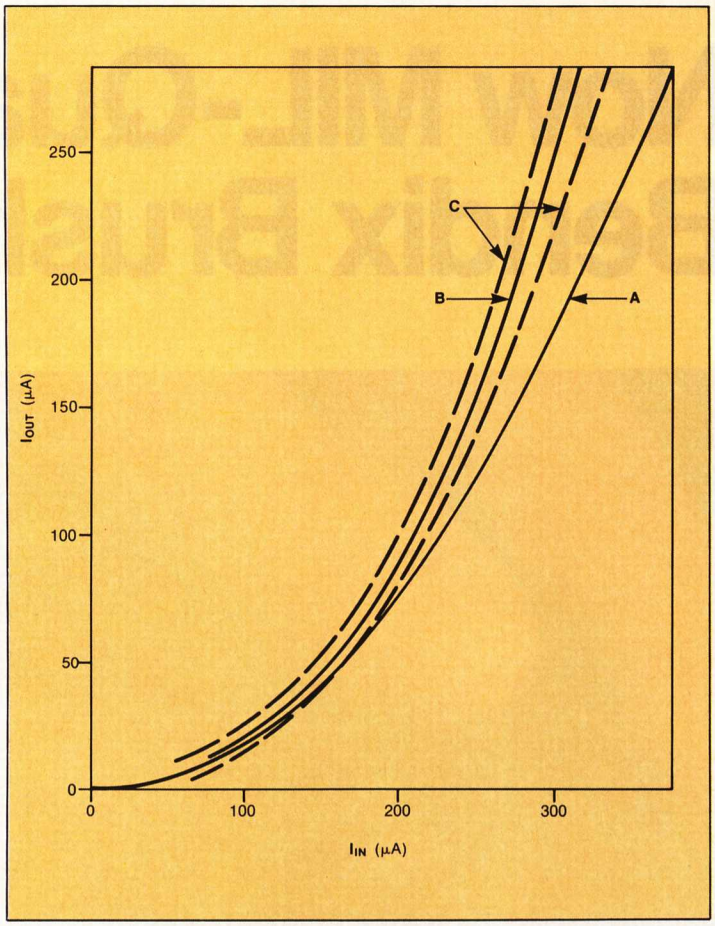

Fig 2—These curves illustrate *the performance of* ***Fig 1****'s circuit. The curve labeled A represents the ideal squaring function, the curve labeled B shows the calculated function, and the two curves labeled C form an envelope for the results obtained using five different CA3096 arrays.*

To Vote For This Design, Circle No 746

Sampling phase detector simplifies a PLL

Russell Kautz
Texas Instruments, Plano, TX

Phase-locked loops can include an analog frequency-mixing circuit (**Fig 1a**) or a digital divider (**Fig 1b**) to accomplish synchronous down-conversion of the reference and input frequencies. An alternative, the sampling system in **Fig 1c**, reduces parts count and cost by a factor of eight. Moreover, the sampling approach removes frequency-conversion circuitry from the signal