IC_1 and IC_2 convert the reference and local-oscillator (LO) frequencies to digital signals. The 2-to-4-line demultiplexer IC_3 then samples these frequencies at 800 Hz (every 1.25 msec). The reference and LO frequencies may differ, but each must be an integral multiple of the sampling rate if the system is to achieve lock.

To set the sampling period, IC_{4A} and IC_{4B} wait for the output 110000110101 (count of 3125) from the 12-bit counter IC_5. When that output occurs, IC_{4C} issues a brief positive pulse that resets the counter and toggles the flip-flop IC_6.

Fig 3 illustrates the digital phase detection that the IC_3 demultiplexer performs. The presence of Y_1 indicates a phase lead between the LO and reference frequencies, and the duration of Y_1 indicates the amount of phase lead. Similarly, Y_2 indicates phase lag. Y_3 goes high when both inputs are high, which ends the sample period by setting the flip-flop.

Note that in **Fig 2** C_1 and C_2 convert the Y_1 and Y_2 pulses to voltage inputs for the differential amplifier IC_8. The amplifier in turn produces a dc voltage representing polarity and magnitude of the local oscillator's phase error. When locked, the loop produces narrow Y_1 and Y_2 pulses (less than 1 nsec) of equal magnitude and duration. The amplifier rejects common-mode signals such as digital noise from the demultiplexer. **EDN**

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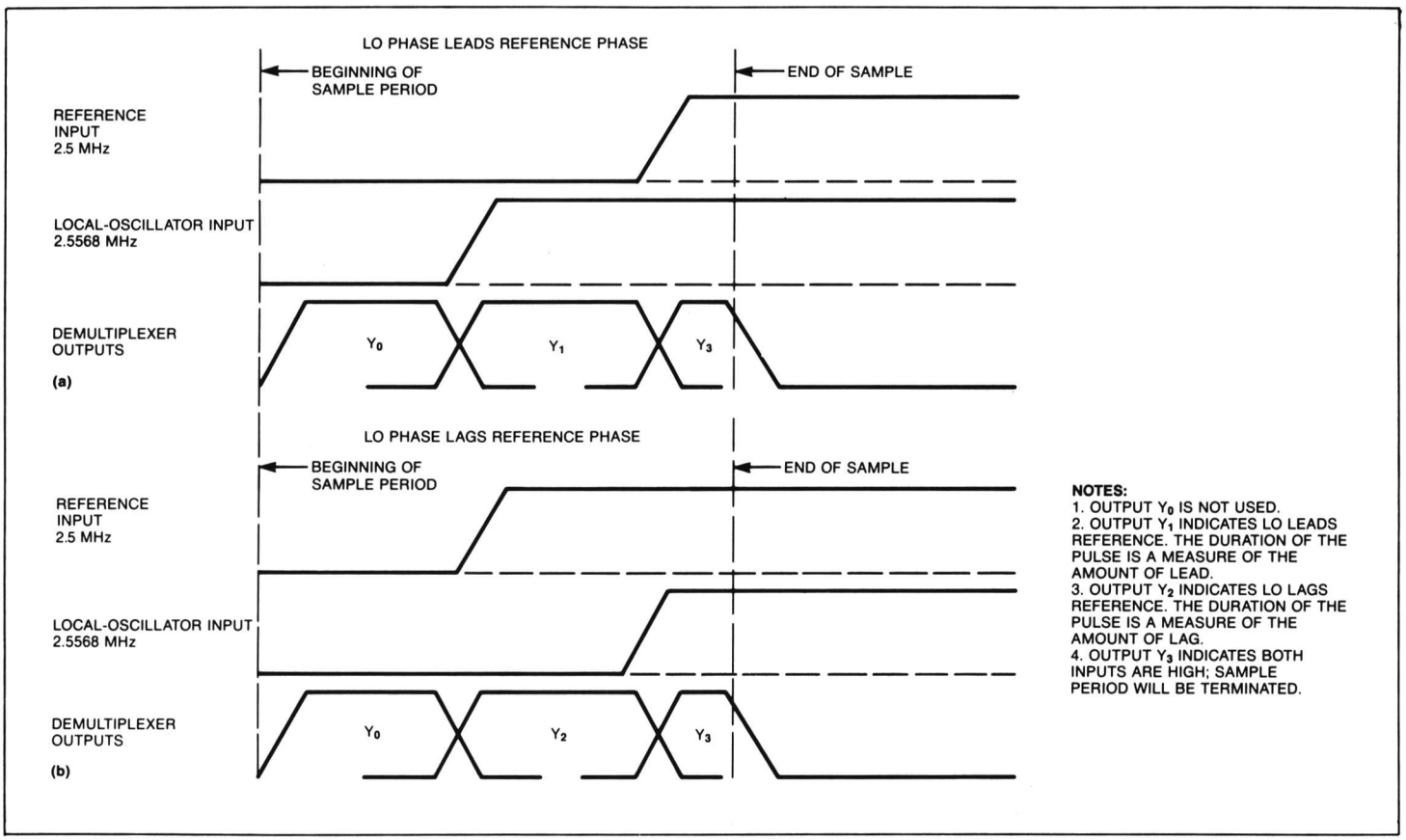

Fig 3—These waveforms depict Fig 2's operation *for the cases of leading phase* ***(a)*** *and lagging phase* ***(b).***

Programmable integrator has 6-decade range

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The voltage-controlled integrator of **Fig 1** provides a programmable time constant for use in applications such as programmable oscillators and programmable filters. Compared with designs based on OTAs (operational transconductance amplifiers) and monolithic multipliers, this circuit offers lower distortion, lower noise gain vs frequency, and better dynamic range. Furthermore, the circuit provides continuous remote tuning

and incurs minimal noise-gain problems during tuning. A 1- to 100-kHz oscillator based on state-variable-filter topology, for example, produces −80 dB of distortion at 100 kHz and −95 dB at 1 kHz (THD plus wideband noise).

The differential control voltage CV sets the time constant of this noninverting integrator. The resulting output is

$$V_{OUT} = \int_0^t V_{IN}dt[\log^{-1}(\log V_{IN} + V_C)],$$

where

$$V_C = \frac{200CV^+}{R_X + 100}.$$

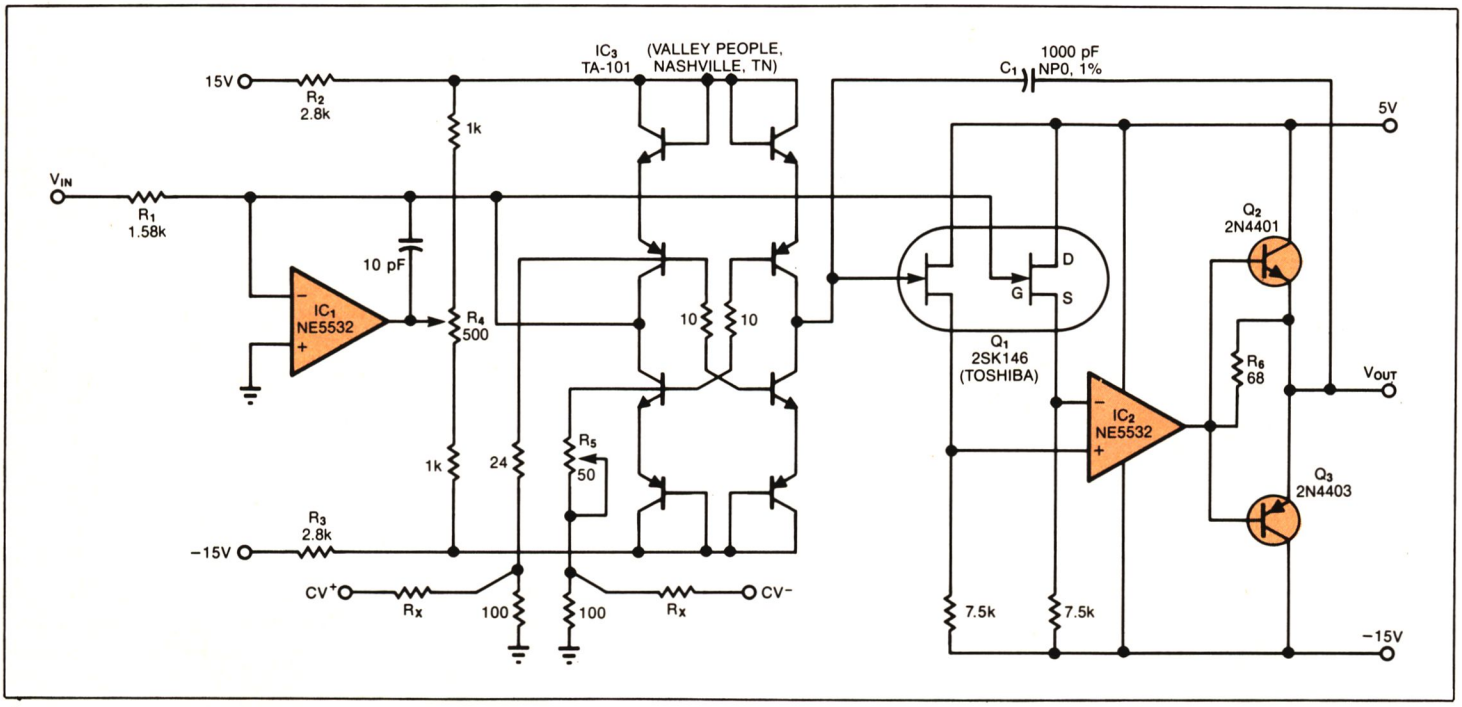

Fig 1—This noninverting integrator *has a voltage-programmable time constant that you can adjust over six decades by varying the differential control voltage CV.*

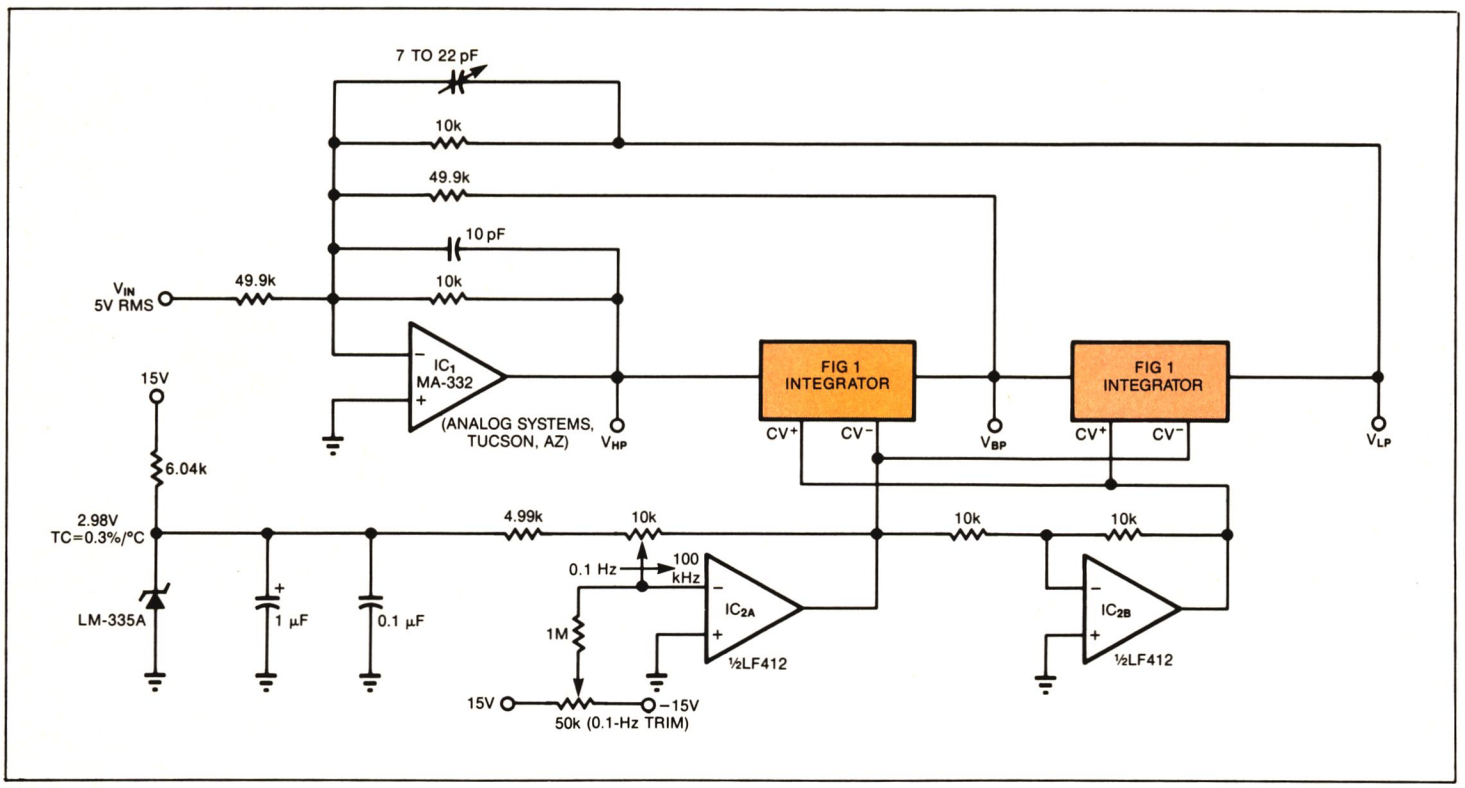

Fig 2—This 0.1- to 100-kHz filter uses two of Fig 1's integrator circuits *and includes an LM-335A temperature sensor to compensate for the transistor array's 3300-ppm/°C temperature coefficient. You set the filter's cutoff frequency by adjusting the 10-kΩ potentiometer.*

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The integrator includes an 8-transistor array connected as a complementary, cross-balanced, log-antilog multiplier. Resistors R_2 and R_3 set a 4-mA bias for the multiplier that allows low-distortion operation for inputs as high as 5V rms and 100 kHz. You trim the circuit for minimum second-harmonic distortion by adjusting R_5 at the highest operating frequency (CV=0V). Then, use R_4 to adjust for minimum distortion at the lowest operating frequency.

You scale the differential control voltage CV^+/CV^- by selecting R_X (two resistors) to provide the desired internal voltage range (a differential of 120 mV at the top of the 100Ω resistors causes one decade of frequency change). CV=0V produces the highest operating frequency allowed by the integrator components R_1 and C_1, which is 100 kHz for this circuit.

The matched pair of JFET source followers (Q_1) buffers the input bias currents of op amp IC_2 and reduces output noise within the integrator's 120-dB operating range. Q_2, Q_3, and R_6 buffer IC_2's output, allowing the integrator to maintain low distortion while driving capacitor C_1 and the output load.

Feedforward compensation (the connection from Q_1 to the virtual ground of IC_1) achieves a threefold increase in Q as compared to that of a simple Miller integrator. In addition, feedforward compensation counters the unwelcome Q enhancement that would otherwise occur in this circuit when used in topologies such as state-variable filters.

The transistor array exhibits a TC of 3300 ppm/°C, for which a thermistor (for example, Tel Labs' Q-81 or EQ) usually provides compensation. However, the thermistor's nonlinear TC and the difficulty of achieving tight thermal coupling between the thermistor and the array make the use of a thermistor troublesome. You can achieve more precise compensation by using an LM-335A temperature sensor as shown in **Fig 2.** The sensor's 2-mA bias generates the same self-heating effect as that experienced by the array. Compensation is quite effective if you protect the sensor from air currents and provide good thermal contact between the sensor and the array. **EDN**

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