ural" or "Napierian" range (NR). This range is defined as the incremental flight distance required for air drag to reduce velocity by a factor of "e," where "e" is the familiar Napierian logarithm base = 2.71828....

Interestingly, $D_P = V^2/NR$. Computation of NR is easiest if the TOF is measured over two ranges in a ratio of 2:1. Let "near" = the near target range (ft), "t_N" = the TOF to the near target, and "t_F" = the TOF to the far target. Note that $t_F > 2t_N$, since air drag continuously slows the projectile during its flight, so flying twice as far takes longer than twice the time.

$$NR = near / \log((t_F/t_N) - 1).$$

With the Napierian range NR (ft) in hand, MV (ft/s) and BC become available as:

$$MV = NR / (t_N(e^{(near / NR)} - 1))$$

$$BC = NR / 24{,}000.$$

The concepts presented here are particularly useful for the calibration of BC and MV in air rifles. By shooting alternately over the two target ranges, accurate values for BC and MV are quickly acquired. This enables realistic trajectory prediction using any of several ballistic software packages. This is helpful in preparation for long-range marksmanship competitions.

Subsequent to finishing this project, it was brought to the author's attention that the seminal idea of acoustic measurement of airgun projectile TOF was previously described in The Air Gun from Trigger to Muzzle, *G.V. Cardew, G.M. Cardew, and E.R. Elsom, Martin Brothers (Printers) Ltd., Birmingham, May 1976.*

Measurement Circuit Features High Common-Mode Rejection

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CIRCLE 521

Modern measurement systems often operate with single 5-V power supplies, yet their input signals may have large common-mode voltages that exceed the supply by tens or hundreds of volts. Also, unless the converter is driven differentially, the noise on the analog-to-digital converter (ADC) reference pin is indistinguishable from a real signal.

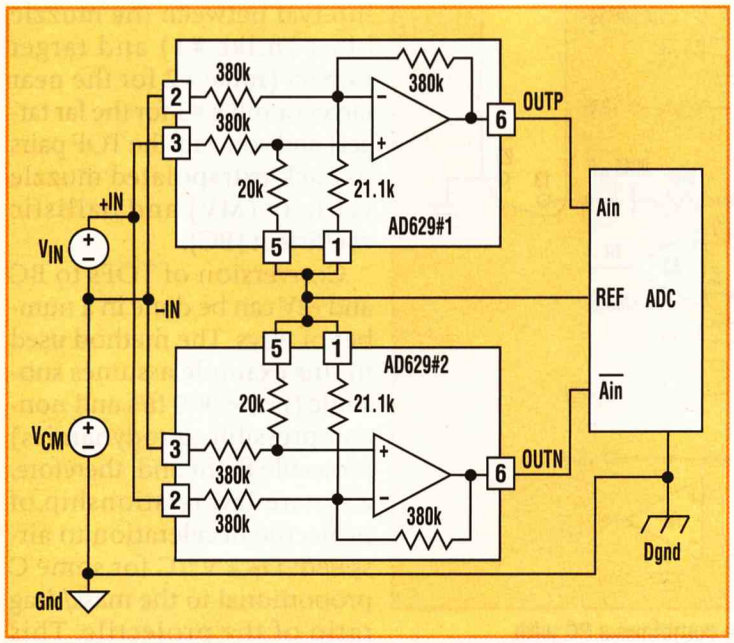
The circuit of Figure 1 solves both of these problems. It provides a gain of 2, along with differential inputs and a differential output. The ADC reference sets the output common-mode level. The amplifier is constructed with two subtractors, each compliant to high common-mode voltage. These subtractors are set up so that the positive input of one connects to the negative input of the other, and vice versa. Their reference pins are tied together and connected to the ADC's reference pin.

As the input signal increases, one output, OUTP, increases, while the other output, OUTN, decreases. Both outputs remain centered with respect to the common-mode level set by the ADC's reference.

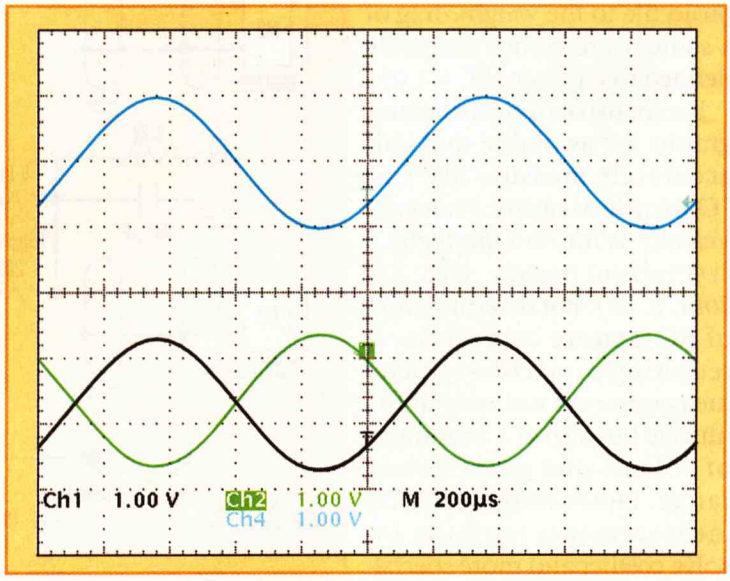
Figure 2 illustrates the circuit's performance with a single 5-V power supply. At the top is a 1-kHz, 2-V p-p input signal. At the bottom are the two outputs in antiphase to produce a 4-V p-p signal centered around the 2.5-V reference.

Figure 3 demonstrates the system's ability to reject a 1-kHz, 60-V p-p common-mode signal. The upper waveform shows the common-mode input, while the lower waveform shows the output.

Bigger power supplies, such as ±15 V,

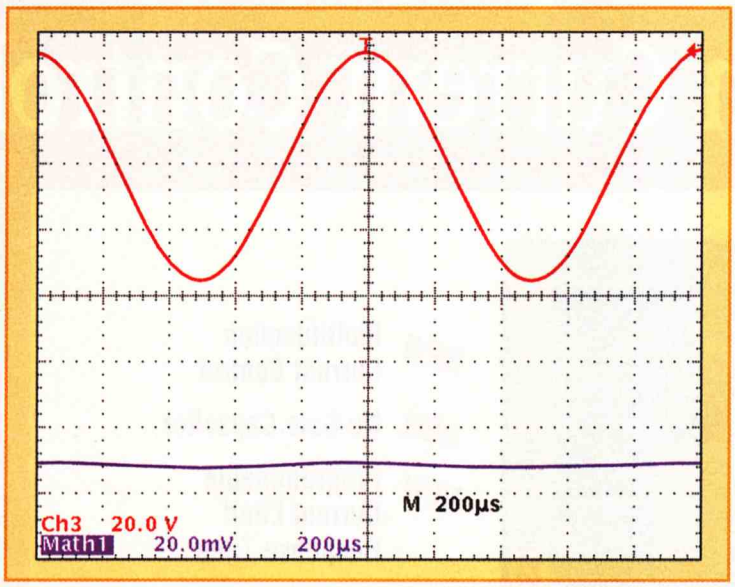


1. Based on two single-supply amplifiers and an ADC, this circuit can measure small signals in the presence of high common-mode voltages.

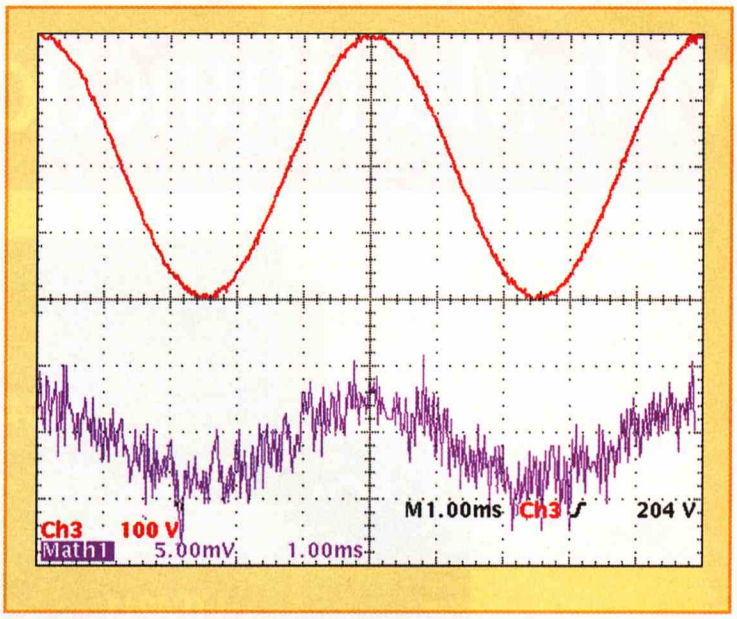


2. These waveforms show circuit performance with a single 5-V supply. The upper trace is the 1-kHz, 2-V p-p input signal, while the lower trace shows the two antiphase outputs, which produce a 4-V p-p signal centered around 2.5 V.

can be used for larger common-mode signals. Figure 4 shows that the system can reject a 400-V p-p common-mode signal (upper waveform), with the residual error of less than 10 mV p-p shown in the lower waveform.



3. With a 5-V power supply and a 1-kHz, 60-V p-p common-mode signal (upper trace), the circuit's output (lower trace) illustrates the high common-mode rejection.



4. Using a ±15-V supply, the circuit reduces a 400-V p-p common-mode signal (upper trace) to under 10 mV p-p (lower trace).

Simple Technique Generates Precise HART Waveforms

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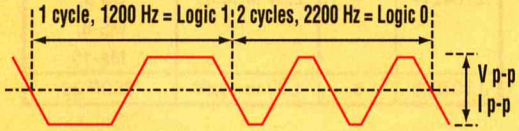
CIRCLE 522

Designed to complement conventional 4- to 20-mA analog signaling, the Highway Addressable Remote Transducer (HART) protocol supports two-way digital communications for process measurement and control devices. The protocol uses frequency-shift keying (FSK), with the digital signal made up of two frequencies—1200 Hz representing ones and 2200 Hz representing zeros. Because the average FSK-signal value is always zero, the 4- to 20-mA analog signal isn't affected.

Ideally, sinewaves of these two frequencies would be superimposed on the dc analog signal to provide simultaneous analog and digital communication. However, generating phase-continuous FSK sinewaves is not a simple matter. So the HART physical-layer specification allows for a more generalized waveform whose shape, amplitude, and rate-of-change must fall within defined limits. A trapezoidal waveform well suits the application *(Fig. 1)*. The limiting values of the parameters are detailed in the table.

The circuit shown in Figure 2 provides a low-cost solution for generating the HART waveform and superimposing it onto a variable dc level. The HART FSK signal fed to the first NAND is gated by the active-high ENABLE signal.

Resistors R4 and R5 split the 5-V rail to form a 2.5-V reference potential, V_{REF}. When ENABLE is low, IC1b's output is low, IC1c's output is high, and because R1 = R2, and assuming the NAND outputs swing rail-to-rail, the voltage V_{IN} at IC2a's noninverting input also sits at 2.5 V.



Parameter	Minimum value	Maximum value
V p-p (V)	0.4	0.6
I p-p (mA)	0.8	1.2
Rate of change at 1200 Hz	1 V/ms (2 mA/ms)	4 V/ms (8 mA/ms)
Rate of change at 2200 Hz	2 V/ms (4 mA/ms)	4 V/ms (8 mA/ms)

1. A typical HART trapezoidal waveform is defined by the parameters shown in the table.

When ENABLE is taken high, the outputs of IC1b and IC1c oscillate in phase with each other and invert the FSK squarewave, such that V_{IN} is now a small squarewave swinging symmetrically about V_{REF} with a peak-to-peak amplitude (in volts) given by:

$$V_{IN(P-P)} = V_P \times \frac{R3}{R3 + R1 \,||\, R2}$$

where V_P is the positive supply-rail voltage, nominally 5 V, and R1||R2 is the parallel combination of R1 and R2. With the resistance values shown in the figure, $V_{IN(P-P)}$ is 200 mV—i.e., the signal swings from 2.4 V to 2.6 V.

At the instant that V_{IN} rises to 2.6 V, IC2a's output goes into positive saturation and C3 starts to charge via R6 and R7. Therefore, the voltage V_{HART} on C3 rises linearly until it reaches 2.6 V. At this point, IC2a rapidly comes out of saturation and behaves as a simple follower, holding V_{HART} at 2.6 V.

When V_{IN} falls to 2.4 V, IC2a's