the count is 00 at power-up. You decode the outputs of the counter with a 2-to-4 line decoder (IC_4) to select one of the output lines, $\bar{0}$ through $\bar{3}$. The outputs of the decoder provide wave drive or 2-phase drive.

Wave drive has one phase on at any given time, and the phases are energized sequentially. **Fig 2a** shows the state table for wave drive. The outputs of the decoder are inverted to turn on the power amplifiers for each phase.

In 2-phase drive, two phases are on at any given instant. The state table for 2-phase drive is shown in **Fig 2b**. To derive the driving sequence for this mode, the outputs are combined two at a time as inputs to the exclusive-OR gates. The gate outputs are connected to the power-amplifier inputs. The power amplifier for one phase is shown in **Fig 3**. **EDN**

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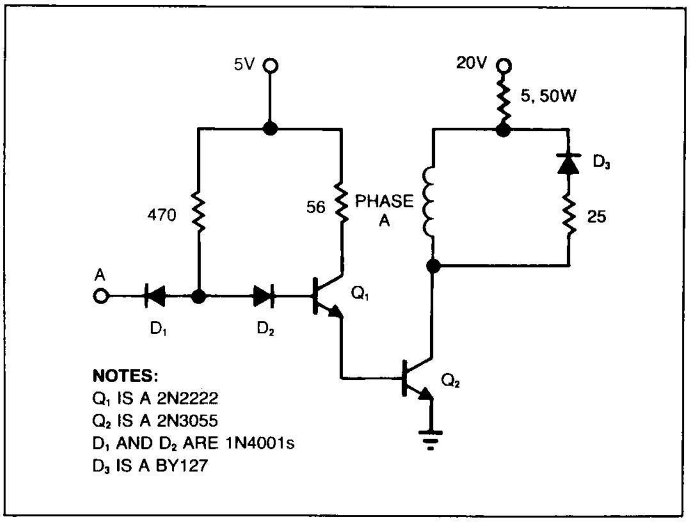

Fig 3—You'll need one of these power amplifiers *for each phase of your stepper motor. Choose Q_2 to reflect the drive requirements of your motor.*

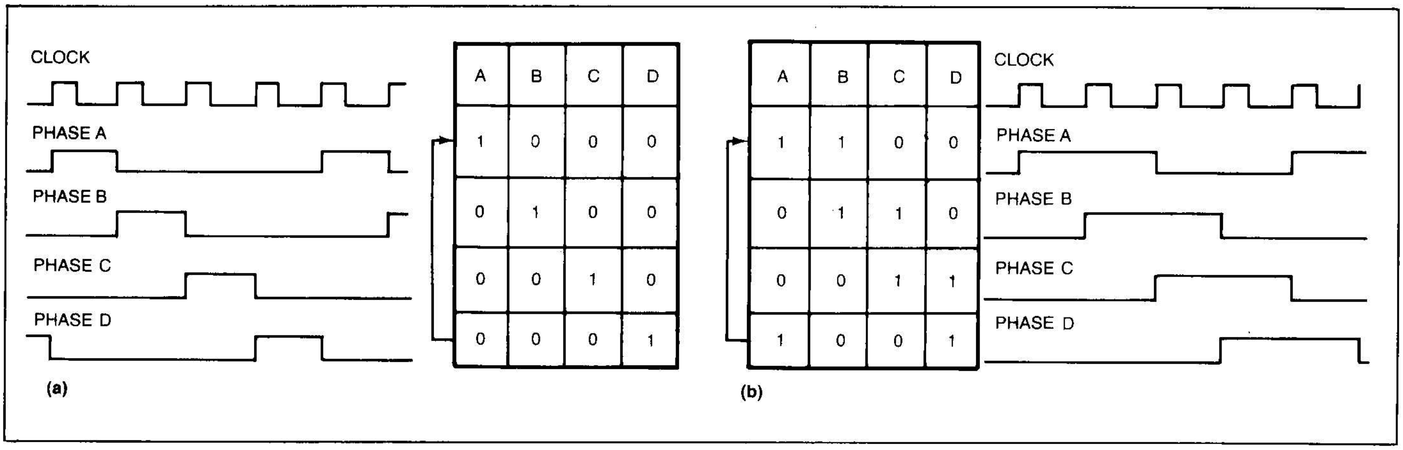

Fig 2—State tables and drive waveforms *depict simple control schemes for 1-phase* ***(a)*** *and 2-phase* ***(b)*** *stepper motors.*

Enhanced op amp delivers 100V p-p

Barry Kline
Technicare Corp, Solon, OH

If you need an amplifier that provides more than ±50V output swing along with the high gain and low offset of a high-performance op amp, consider the **Fig 1** circuit. It employs a gain stage (Q_1-Q_4, R_1-R_4) to multiply the op amp's ±10V output swing to the desired level. The combined op amp and gain stage may be regarded as a high-voltage amplifier.

The gain stage is based on a design by Jerald Graeme (**Ref 1**), but adds current feedback via R_4 to achieve three performance improvements: reduction of open-loop output impedance (reduced sensitivity to changes in load current); reduction of output current I_A from the op amp; and increased dynamic range due to a reduction in signal voltage across the current-sensing resistors R_{1A} and R_{1B}.

Q_1 and Q_3 act as cascode stages for the op-amp supply currents I_{A1} and I_{A2}. Q_2 and Q_4 sense these currents and provide amplified output currents I_1 and I_2:

$$I_{O1} = I_{A1} \times \frac{R_1}{R_2}$$
$$I_{O2} = I_{A2} \times \frac{R_1}{R_2} \qquad (1)$$

Also, because the difference in supply currents is equal to the op-amp output current ($I_A = I_{A1} - I_{A2}$),

$$I_{O1} - I_{O2} = (I_{A1} - I_{A2}) \times \frac{R_1}{R_2} = I_A \times \frac{R_1}{R_2}. \qquad (2)$$

Feeding this current imbalance back to the op-amp output terminal provides negative feedback for the booster stage. Recall that:

$$I_{O1} - I_{O2} = I_A \times \frac{R_1}{R_2}. \qquad (3)$$

In addition,

$$I_4 = (I_{A1} - I_{A2}) - I_L = \left(I_A \times \frac{R_1}{R_2}\right) - I_L.$$

$$\text{But,}\quad I_A = I_3 - I_4.$$

$$\text{So,}\quad I_4 = (I_3 - I_4) \times \left(\frac{R_1}{R_2}\right) - I_L. \qquad (4)$$

$$\text{Or,}\quad I_4\left(1 + \frac{R_1}{R_2}\right) = \left(I_3 \times \frac{R_1}{R_2}\right) - I_L.$$

Substitute V_A for the op amp's output voltage:

$$I_4 = \frac{V_{OUT} - V_A}{R_4}$$

$$I_3 = \frac{V_A}{R_3} \qquad (5)$$

$$I_L = \frac{V_{OUT}}{R_L}.$$

Therefore:

$$\frac{V_{OUT} - V_A}{R_4}\left(1 + \frac{R_1}{R_2}\right) = \frac{V_A R_1}{R_3 R_2} - \frac{V_{OUT}}{R_L}. \qquad (6)$$

The equation can be solved for voltage gain of the booster stage:

$$\frac{V_{OUT}}{V_A} = \frac{1 + \frac{R_4}{R_3}\left(\frac{R_1}{R_1 + R_2}\right)}{1 + \frac{R_4}{R_3}\left(\frac{R_2}{R_1 + R_2}\right)} \qquad (7)$$

$$= 1 + \frac{R_4}{R_3}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_L}{R_O + R_L}\right).$$

Output impedance (R_O) is:

$$R_O = \frac{R_4 \times R_2}{R_1 + R_2}. \qquad (8)$$

To calculate the op amp's output current (I_A):

$$I_A = I_3 - I_4 = \frac{V_A}{R_3} - \frac{V_{OUT} - V_A}{R_4}$$

$$= V_A\left(\frac{1}{R_3} + \frac{1}{R_4} - \frac{V_{OUT}}{V_A R_4}\right). \qquad (9)$$

The no-load booster gain is obtained by setting R_L to infinity in **Eq 7**:

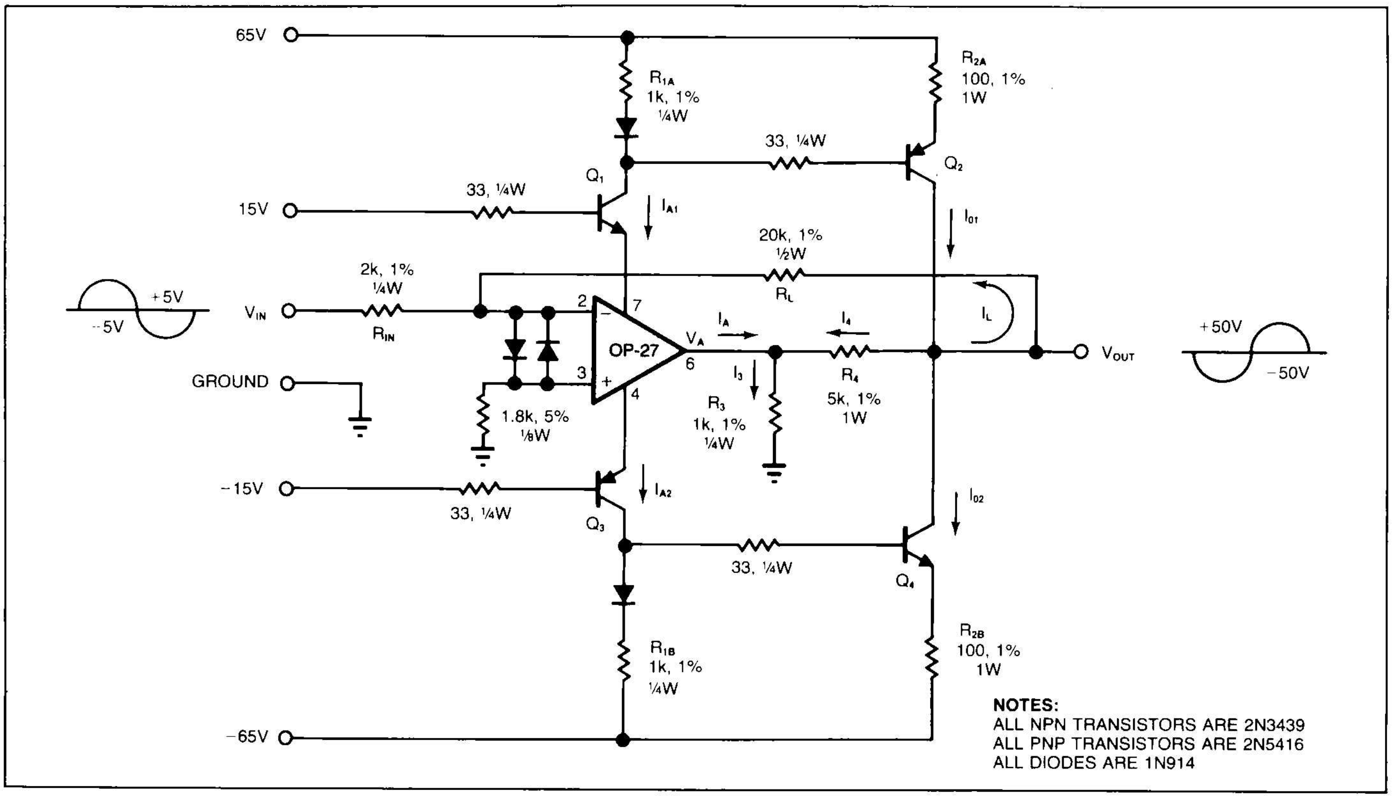

Fig 1—Gain stage with current feedback *boosts a conventional op amp's output to more than 100V p-p.*

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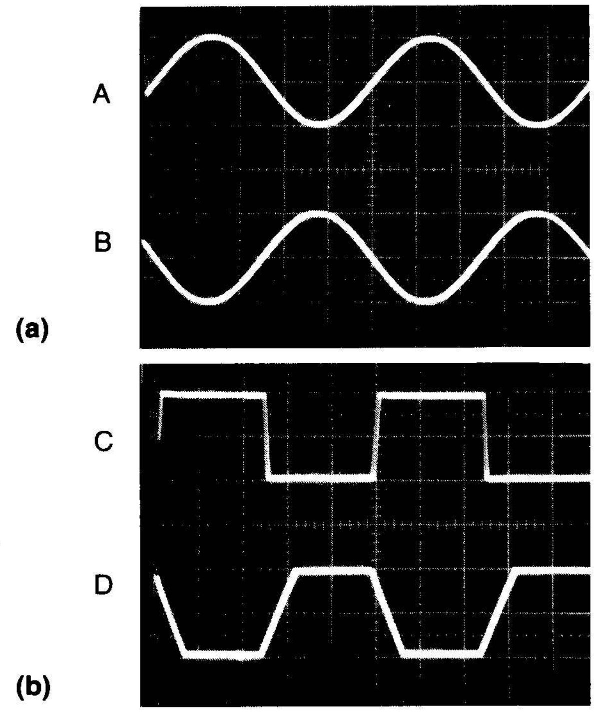

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	10 μSEC/DIV
B	50V/DIV	10 μSEC/DIV
C	5V/DIV	10 μSEC/DIV
D	50V/DIV	10 μSEC/DIV

***Fig 2—The Fig 1 circuit produces 100V p-p** sine- and square-wave outputs—**a** and **b**, respectively. Slew response to the square wave is a product of the OP-27 slew rate (2.8V/μsec typ) and gain of the booster stage (approximately 5.5).*

$$\frac{V_{OUT}}{V_A} = 1 + \frac{R_4}{R_3}\left(\frac{R_1}{R_1 + R_2}\right). \qquad (10)$$

Substituting the **Eq 10** no-load booster gain into **Eq 9** yields:

$$I_A = \frac{V_A}{R_3}\left(\frac{R_2}{R_1 + R_2}\right) \qquad (11)$$

The use of current feedback reduces the output impedance and the required op-amp output current by a factor of $R_2/(R_1+R_2)$. Also, reducing I_A reduces signal current variations in the supply lines.

Be careful not to exceed the power-dissipation capacity of components Q_2, Q_4, R_2, R_4, and R_L. In addition, quiescent current in Q_2 and Q_4 is proportional to the current gain R_1/R_2, so choose this ratio carefully. **EDN**

Reference

1. Graeme, Jerald G, *Designing with Operational Amplifiers—Applications Alternatives*, McGraw-Hill, 1977, pg 14.

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was mandated by the government because (statistically) it helps to reduce the number of rear-end collisions.

Yes, I am all for the use of modern technology and mathematics to build safer, more efficient, and more reliable cars. Mr Bismarck should open his closed mind and take another look at this technology.

Sincerely,
N Paul Galluzzi, EE
Dynamics Research Corp
Wilmington, MA

Corrections

Please note the following corrections to two equations in the Design Idea "Enhanced op amp delivers 100V p-p" by Barry Kline (EDN, September 5, pg 309). **Eq 4** on pg 311 should read:

$$I_4 = \left(I_{O1} - I_{O2}\right) - I_L$$
$$= \left(I_A \times \frac{R_1}{R_2}\right) - I_L.$$

Eq 7 should read:

$$\frac{V_{OUT}}{V_A} = \frac{1 + \frac{R_4}{R_3}\left(\frac{R_1}{R_1 + R_2}\right)}{1 + \frac{R_4}{R_L}\left(\frac{R_2}{R_1 + R_2}\right)}$$

$$= \left[1 + \frac{R_4}{R_3}\left(\frac{R_1}{R_1 + R_2}\right)\right]\left(\frac{R_L}{R_O + R_L}\right).$$

In addition, in the Design Idea "Detect out-of-bound pulse widths" by Dil Sukh Jain (EDN, September 19, pg 242), the statement "Each NAND-gate output is high unless either or both inputs are low" is incorrect. The statement should read: "Each NAND-gate output is high when either or both inputs are low." Also, in IC_{1b} in Fig 1, Q_2 should be $\overline{Q_2}$.

Finally, in the Design Idea entitled "Switch lets you select memory devices" (EDN, July 25, pg 312), the authors' names appeared in reverse order. The article was contributed by D V Poornaiah and M O Ahmad, in that order.