DC Feedback Stabilizes Bias On FET/Bipolar Pair

Simple voltage-feedback loop stabilizes bias on direct-coupled FET and bipolar stages.

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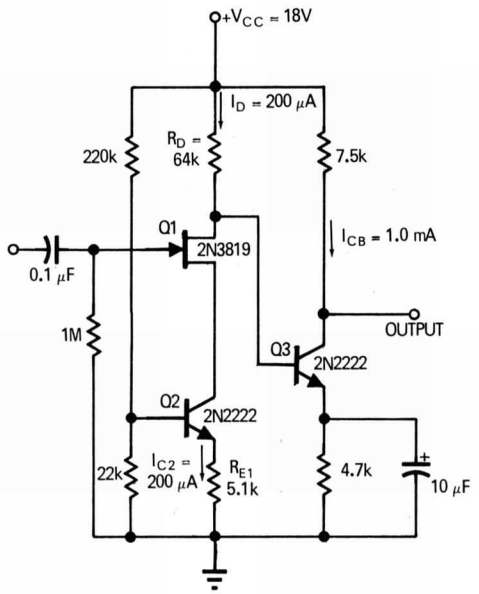
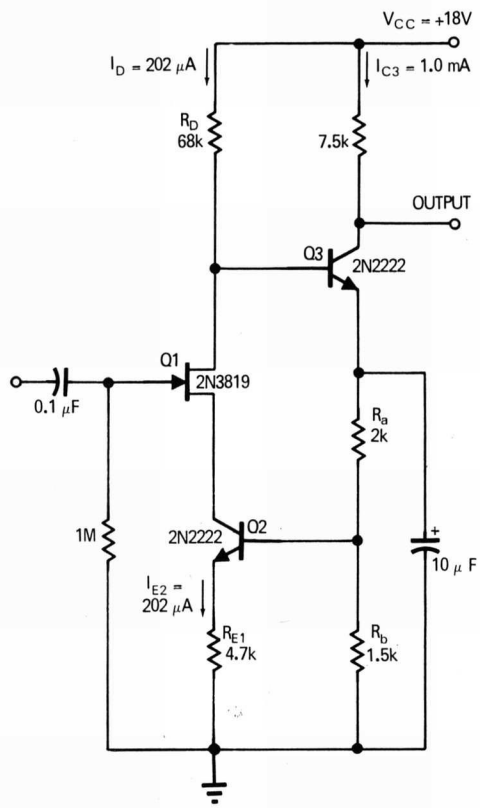
Direct coupling a FET to a bipolar transistor involves the problem of how to make the FET bias the bipolar correctly. This problem results from the fact that current through the FET depends on the device parameters (I_{DSS}, V_P) and source resistance. Correct dc coupling to the bipolar requires that the FET be biased properly.

There are several methods of biasing a FET independently of its parameters. Supplying the source terminal with a constant current is one method. A constant current forced through the drain sets the bias voltage at the base of the bipolar. However, drift in the constant-current source shifts this voltage and "unbiases" the bipolar.

A possible solution to this problem is to make the constant-current source dependent on the bipolar bias current. By choosing proper resistor values, dc voltage feedback from the emitter of the bipolar can be made to control the constant current value. Since this current nearly equals the FET drain current, the base-bias voltage of the bipolar is set at its desired value. Any change in drain current causes an opposite change in the constant-current value, thus stabilizing the bipolar. □



Unstable biasing method for FET Q1 direct coupled to bipolar transistor Q3. Constant-current source Q2 properly biases FET Q1 independently of its parameters I_{DSS} and V_P. Constant-current source Q2 determines FET drain current I_D and sets bias voltage at Q3 base. However, drift in Q2 collector current I_{C2} shifts base-bias voltage causing instability.



Stable Biasing Method incorporates dc-voltage feedback from Q3 emitter to base of constant-current stage Q2 to maintain stable bias voltage at Q3 base. Any change in Q2 collector current is reflected as an opposite change in Q3 collector (and emitter) current. Voltage divider R_a, R_b adjusts Q2 base voltage to restore the original current value. Feedback method maintains stable bias on Q3. Design equation for Q3 collector current is:

$$I_{C3} = \frac{V_{CC} - V_{BE3} + \frac{R_D}{R_{E1}} V_{BE2}}{R_a + R_b \left[1 + \frac{R_D}{R_{E1}}\right]}$$

Collector current thus is a function of resistor values and completely independent of FET parameters. I_{DSS} value ranging from 3 to 20 mA has negligible effect on Q3 collector current.

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