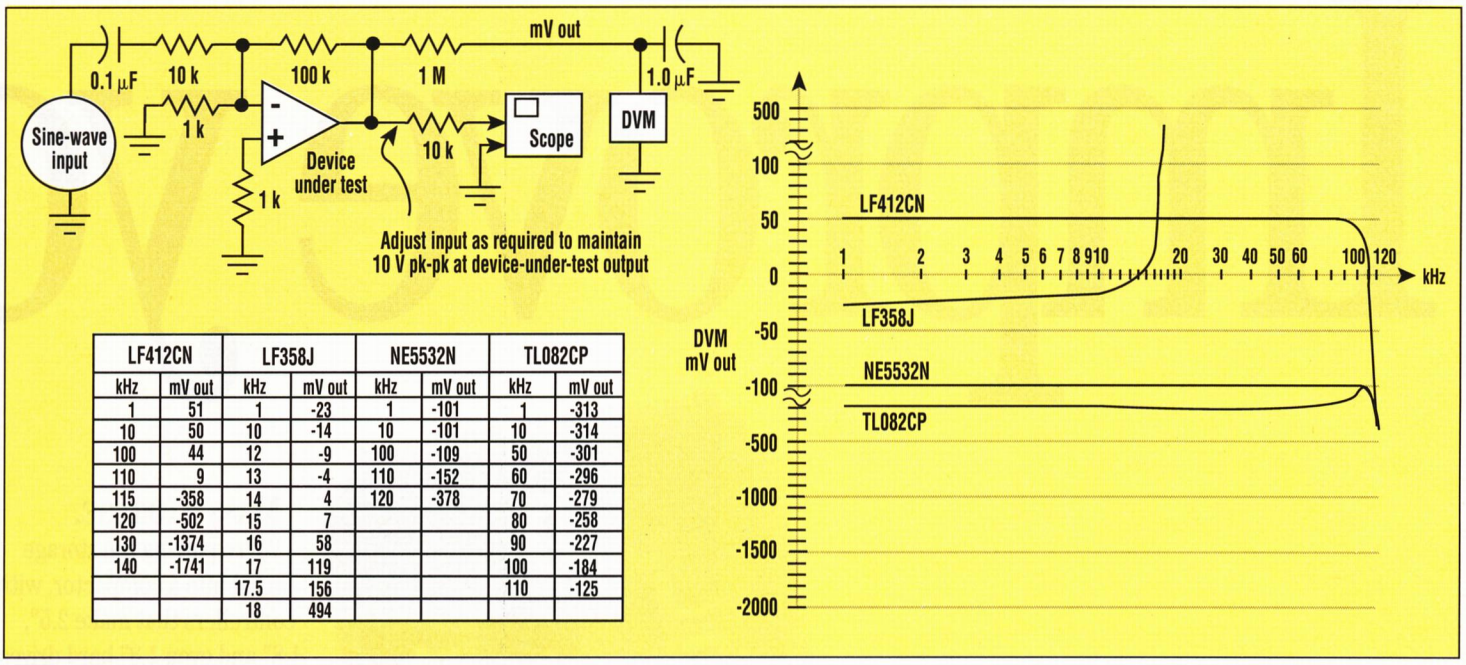

LF412CN		LF358J		NE5532N		TL082CP	
kHz	mV out	kHz	mV out	kHz	mV out	kHz	mV out
1	51	1	-23	1	-101	1	-313
10	50	10	-14	10	-101	10	-314
100	44	12	-9	100	-109	50	-301
110	9	13	-4	110	-152	60	-296
115	-358	14	4	120	-378	70	-279
120	-502	15	7			80	-258
130	-1374	16	58			90	-227
140	-1741	17	119			100	-184
		17.5	156			110	-125
		18	494				

USING THIS SETUP, dc offset shift can be tested. The table and graph show the results obtained with four different devices.

CIRCLE 521

CHECK FOR OP-AMP DC OFFSET SHIFT

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The dc values of op-amp offsets can't always be taken for granted when delivering ac outputs. No device is ever exactly symmetrical for maximum positive slew rate versus maximum negative slew rate. Consequently, there's always some range of output slew rates in which the device used limits in one direction more severely than in the other. What results is rectification of the ac signal and an apparent shift of the dc offset.

This test circuit *(see the figure)* can check for the shift phenomenon. The accompanying table and graph illustrate the results obtained for four devices, all of different types. As frequency and slew rate are increased, the effect can be either relatively abrupt (LF412CN and NE5532N) or relatively gradual (LF358J and TL082CP).□

CIRCLE 522

PLL COMPARES CAPACITORS

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With this simple test circuit *(see the figure, p. 96)*, a given capacitor's (C_X's) value can be instantaneously revealed as being higher, lower, or within the percentage limits compared with a reference capacitor (C_{REF}). As a result, the tester, which is built around the commonly used and inexpensive CMOS PLL CD4046, can be used to select capacitors for use in such circuits as active filters, PLL circuits, tone decoders, and so forth.

Capacitors C_X and C_{REF} decide the ON and OFF periods, respectively, of the square wave at the VCO's output. Integrator R_4C_1 develops a dc voltage proportional to the square wave's duty cycle. Comparators a and b compare the dc voltage against the two adjustable reference levels $V_{REF\text{-}HI}$ and $V_{REF\text{-}LO}$. The three LEDs (two red and one green) indicate the test results.

If capacitor $C_X = 1.01\ C_{REF}$, then the ON period (t_{ON}), OFF period (t_{OFF}), duty cycle (n), and integrator output (V_{INT}) will have the following relationships:

$t_{ON} = 1.01\ t_{OFF}$, $n = 1.01/2.01 = 0.502$, $V_{INT} = nV_{DD} = 6.024$ V

Similarly, for $C_X = 0.99\ C_{REF}$: $t_{ON} = 0.99\ t_{OFF}$, $n = 0.99/1.99 = 0.497$ and $V_{INT} = 5.964$ V

Hence, for a comparison check that is ±1%, the two reference voltages are: $V_{REF\text{-}HI} = 6.024$ V and $V_{REF\text{-}LO} = 5.964$ V.

When tested, it was found that the accuracy for lower capacitor values is limited by the stray capacitance inherent to the circuit. For higher values (lower VCO frequencies), accuracy is limited by the ripple voltage overriding the dc voltage at the integrator's output. The ripple voltage makes two LEDs turn on simultaneously.

During testing, it was found that the device compared capacitors in the range of 100 pF to 10,000 pF for a comparison limit of ±1%.□