PART TWO COMPUTING CIRCUITS

The earliest applications of operational amplifiers were in computational structures applied to indirect modelling, called *analog computors*. In this Part, we present circuits that have found, or are likely to find, their principal employment by members of the computing trade, regardless of their persuasion—analog, digital, or "hybrid." These circuits will readily be seen to have applications beyond the limited scope of problem-solving and data-handling, and a number of the more articulately-rendered circuits in the "instrument" section will be recognized as directly derived from the simple, basic configurations described here.

For convenience, for order, and for other good reasons, this Part has been divided into three sub-plots: *Linear Circuits; Continuous-Function Nonlinear Circuits;* and *Discontinuous-Function Nonlinear Circuits.*

Linear Circuits

Though these circuits are inherently linear (i.e., output magnitudes bear a directly proportional relationship to input magnitudes), bear in mind that they are often used successfully in combination with *non*linear devices and circuitry; either in the same Amplifier circuit, or in league with other Operational Amplifiers. Naturally, no claim to comprehensiveness is made here, either in diversity or in detail, but enough circuits are provided to encourage the Thoughtful Reader to expand on the basic ideas here discovered, and, so armed and stimulated, to crash through to solutions of his specific (and perhaps unique) problems.

Modules II.1-II.21 . . . pages 39–49

Continuous-Function Nonlinear Circuits

If linear circuits are best characterized by their fundamentality and ubiquity, the circuits in this second subdivision are most notable for their *permutability*—the range and diversity of function that may be achieved by combining, superimposing, or reiterating them. Small wonder that we can here give only a representative and —we hope—intelligent sampling of the most powerfully potent of the genre! Once again, many of the seeds planted here will be found flowering in Part III, in the form of Instruments of bold ambition and gratifying competence.

Modules II.22-II.33 . . . pages 50–55

Discontinuous-Function Nonlinear Circuits

Veteran followers of Philbrick publications (a calloused lot) will find nothing remarkable in the generous way in which we embrace such elements of the ungainly Digital Discipline as flipping, flopping, and gating. Indeed, we feel no such reluctance—most of these circuits were born analog—and find themselves in their constricted hysteretical, or schizophrenic condition because they have been driven to their limits . . . accidentally at first, perhaps, but now deliberately. Mad and misshapen though they be, they can be very useful indeed, and we value the end above the means, if the blood lines are right. (Digits are members of the Analog family.)

Modules II.34-II.51 . . . pages 56–62

II.1 UNITY-GAIN INVERTER. A voltage inverter, or one-to-one electronic lever, is formed by using identical impedances in the input and feedback paths. The impedances are usually purely resistive, but sometimes the use of identical reactive or complex impedance elements will improve the overall frequency response.

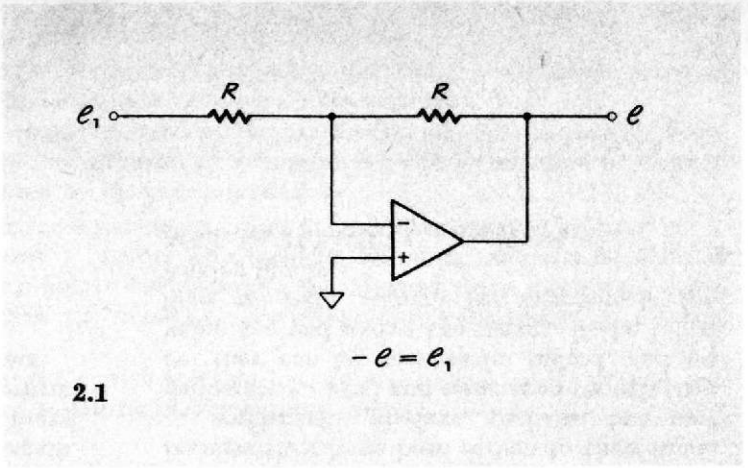
The equation for the inverter response (ideal) may be derived from the general equation (1–4) for this configuration, introduced in I.6, by substituting Z for both Z_1 and Z_2, thus:

$$e = -\frac{Z_2}{Z_1}e_1 = -\frac{Z}{Z}e_1 = -e_1 \qquad (2\text{-}1)$$

Inverters are used wherever sign changes are necessary, or simply to lower the impedance level (and raise the power level) of a signal. In the circuit shown, the output impedance is usually less than an ohm, whereas the input impedance is:

$$Z_{in} = \frac{e_1}{i_{in}} = R \qquad (2\text{-}2)$$

This circuit functions well over a very wide range of impedances, signal levels, and frequencies. Noise, DC offset, and drift determine the minimum practical signal; and amplifier input current, Johnson noise, leakage, bandwidth requirements, and (possibly) pickup limit the maximum value of R.



2.1

II.1
I.5
to
I.7
II.3
II.6
II.9

II.2 THE FOLLOWER. The follower circuit of (a) has essentially unity gain because the output, e, is fed directly back to the negative input as degenerative feedback at high gain. It has very nearly unity gain over a wide frequency range, provided that the amplifier has excellent differential properties and high gain.

The follower is ideal for isolating and driving other circuits, as well as for direct signal detection at low energy . . . and it preserves the sign of the signal (is non-inverting).

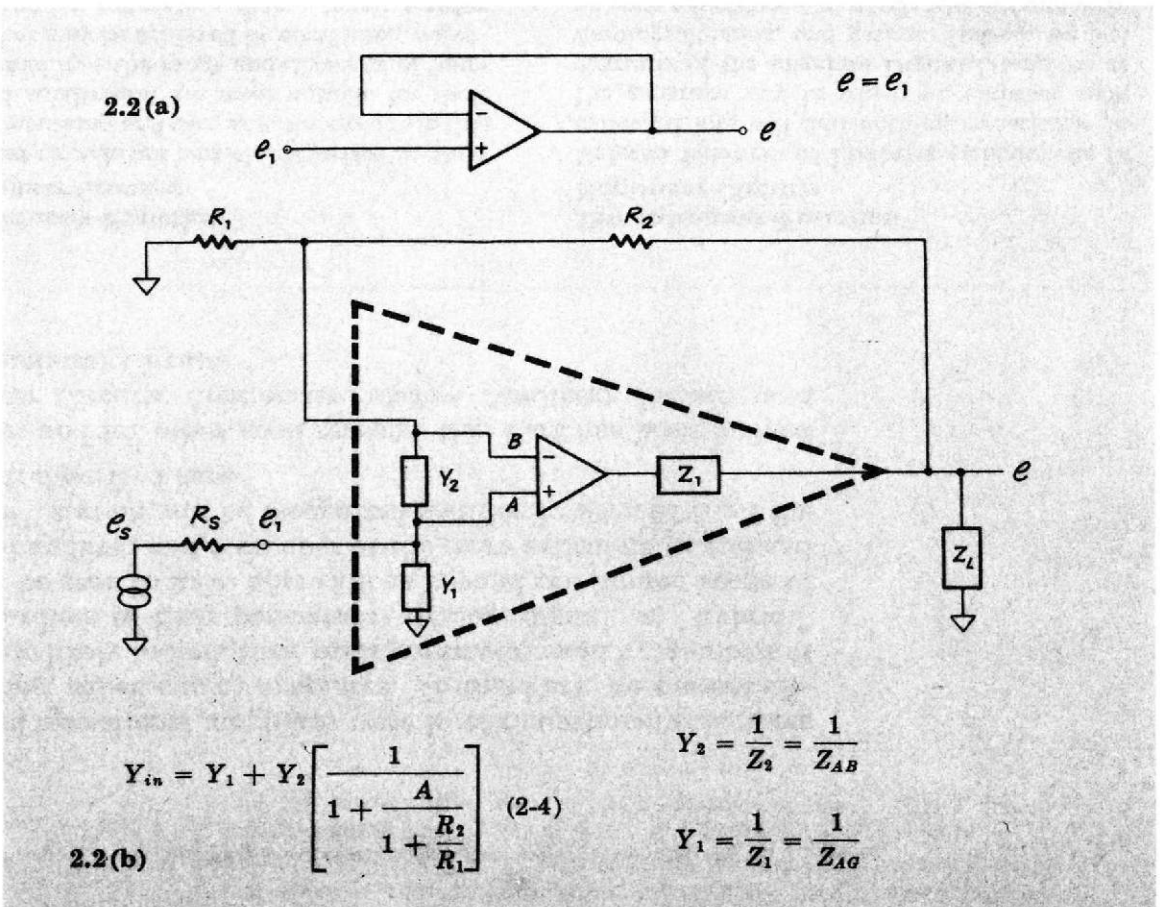
The response of the follower-with-gain circuit (b) is

$$e = \left(1 + \frac{R_2}{R_1}\right)e_1 \qquad (2\text{-}3)$$

Circuit (b) is less demanding of differential excellence, for two reasons. First, for equal outputs, the input (i.e., common-mode) voltage of (b) is smaller. Thus, even a curvilinear relationship between common-mode error and common-mode voltage is correctable, in (b), by trimming gain, assuming the gain is high enough.

Secondly, some differential amplifiers have dynamics that are optimized for inverting work, and, therefore, respond more rapidly to signals applied to the negative input terminal than to the positive. For low values of gain, the positive-input lag rather than the gain-bandwidth product limits the speed of response. Also, output rate-limiting resulting from input saturation is much less a factor in (b), because of the smaller input. For these reasons an amplifier having severe limitations as a unity-gain follower may be excellent as a gain-of-100 follower-amplifier.

The input admittance of (b), for R_1 or $R_2 \ll 1/Y_2$, is given in equation (2-4).



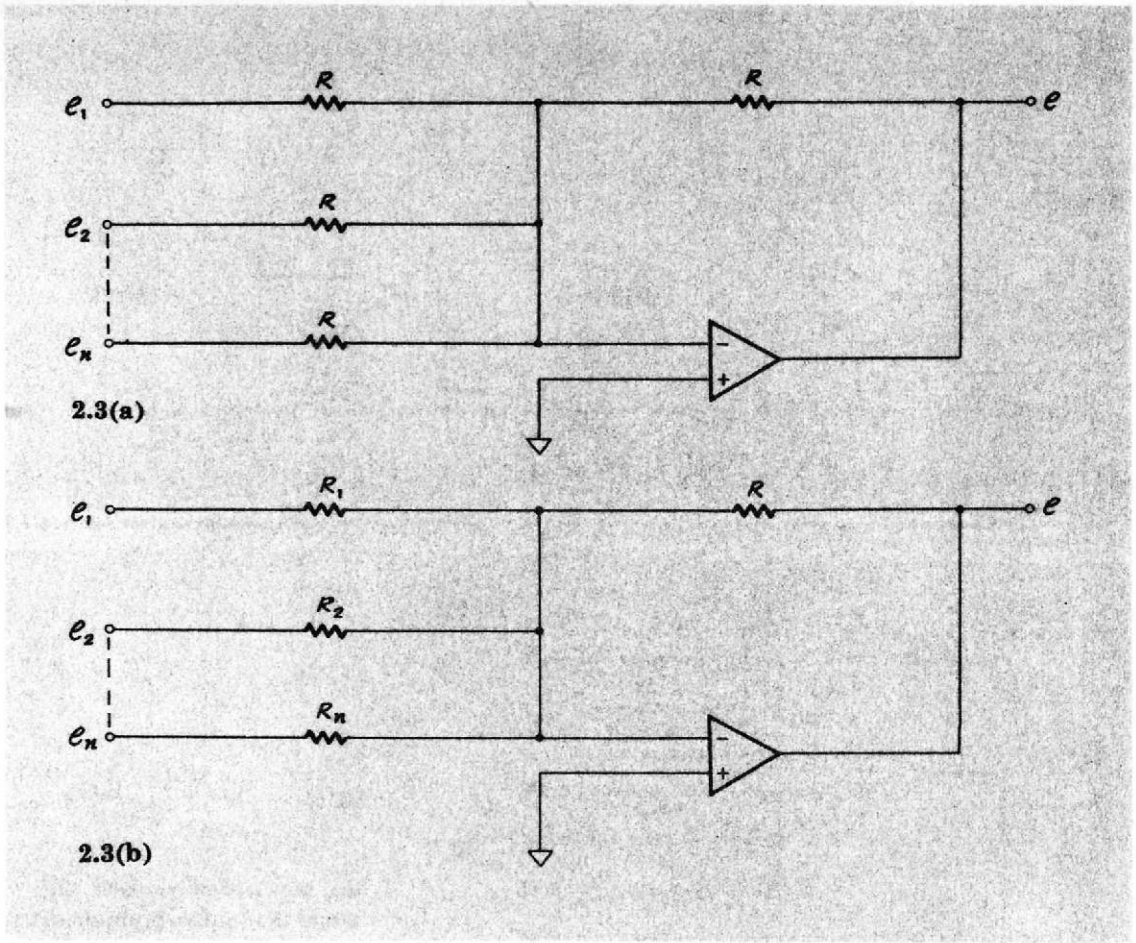
II.2
I.5
to
I.7
I.16
I.18
I.23
III.32
to
III.34

II.3 THE INVERTING ADDER—WITH & WITHOUT WEIGHTING. Circuit (a) adds linearly; that is, when n input voltage signals $e_1, e_2, \ldots e_n$, are applied to the input terminals, the voltage sum is delivered at the output terminal. (See I.7.) When all resistors are equal, the circuit thus acts as a one-to-one inverter with respect to each input to a very high accuracy provided that the amplifier gain is high. The response is given by:

$$\bullet - e = e_1 + e_2 + \cdots + e_n \qquad (2\text{-}5)$$

Circuit (a) is but a special case of the generalized circuit of section I.6, and it immediately suggests other circuits, less general than that of I.6, but more general than (a)—for example, (b), in which the individual input resistors may have values different from that of the feedback resistor, so that the output is the sum of a series of terms, each proportional to one of the input signals, *but each multiplied by an arbitrary coefficient* Thus, in producing a "sum," we may *weight* (or "scale") the inputs arbitrarily, merely by selecting appropriate values of input resistance. Circuit (b) is sometimes called a "Linear Combinor." Its response is given by:

$$-e = e_1\left(\frac{R}{R_1}\right) + e_2\left(\frac{R}{R_2}\right) + \cdots + e_n\left(\frac{R}{R_n}\right) \qquad (2\text{-}6)$$



II.3
I.5
to
I.7
I.18
II.4
to
II.10
II.19
II.23

II.4 THE NON-INVERTING ADDER. The output of this circuit is (ideally) the direct, *positive* sum of the two inputs. In other words, we have constructed a *non*-inverting adder. A brief analysis of this circuit should prove useful, since its fundamental configuration permits a number of interesting variations.

As always, we begin by assuming that e_n is 0, so that the potential with respect to ground at the positive input, e_A, is the same as that at the negative input, e_B. From the proportions of the feedback network connected to the negative input, it is clear that:

$$e_B = e\left(\frac{R}{R+R}\right) = \frac{e}{2} \qquad (2\text{-}7)$$

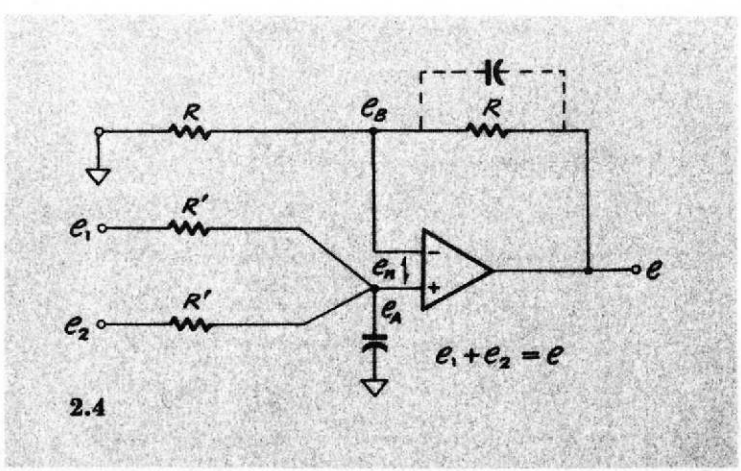
We may also derive an expression for e_A, in terms of e_1, e_2, and the resistance values.

$$\frac{e_1 - e_A}{R'} + \frac{e_2 - e_A}{R'} = 0$$
$$e_1 + e_2 = 2e_A \quad \text{or} \quad e_A = \frac{(e_1 + e_2)}{2} \qquad (2\text{-}8)$$

If the input-terminal potentials are equal,

$$e_A = \frac{e_1 + e_2}{2} = e_B = \frac{e}{2} \text{ or, } e_1 + e_2 = e \qquad (2\text{-}9)$$

This circuit is not limited to two inputs, nor to *simple* addition—the coefficients may be arbitrarily weighted by using appropriate resistor values and some algebra.



II.4
I.5
to
I.7
I.16
I.18
II.3
II.5

II.5 THE NON-INVERTING ADDER/SUBTRACTOR. Only a perverse and unnatural insensitivity could resist exploring the possibility of obtaining *negative coefficients* with some practical form of the preceding circuit, and thus achieving *subtraction* . . . preferably, of course, without compromising the ability of the circuit to add, simultaneously. Circuit (a) satisfies both ambitions. Space does not permit the derivation of the expression for the output voltage, but it can be shown that, *provided that* the following relationship is satisfied:

$$k_1 + k_2 + k_3 = k_4 + k_5 \qquad (2\text{-}10)$$

the response equation is given by:

$$e = k_4 e_4 + k_5 e_5 - (k_1 e_1 + k_2 e_2 + k_3 e_3) \qquad (2\text{-}11)$$

A simple way of "forcing" the provisional relationship is to add a resistor, R/k_0 or R'/k_0, from either the negative terminal of the amplifier or the positive terminal, to ground, depending upon which side of the provisional equation must be made larger to achieve the equality. This resistor, since it is grounded, corresponds to a term of the general form: $k_0 e_0$ in which the voltage, e_0, is zero, and hence does not add a signal term to the basic relationship. If a single input, e_1, is applied to the negative terminal, and a single input, e_2, is applied to the positive terminal, and $k_1 = k_2 = 1$, then the circuit is reduced to a simple subtractor, figure (b), the response of which is:

$$e = e_2 - e_1 \qquad (2\text{-}12)$$

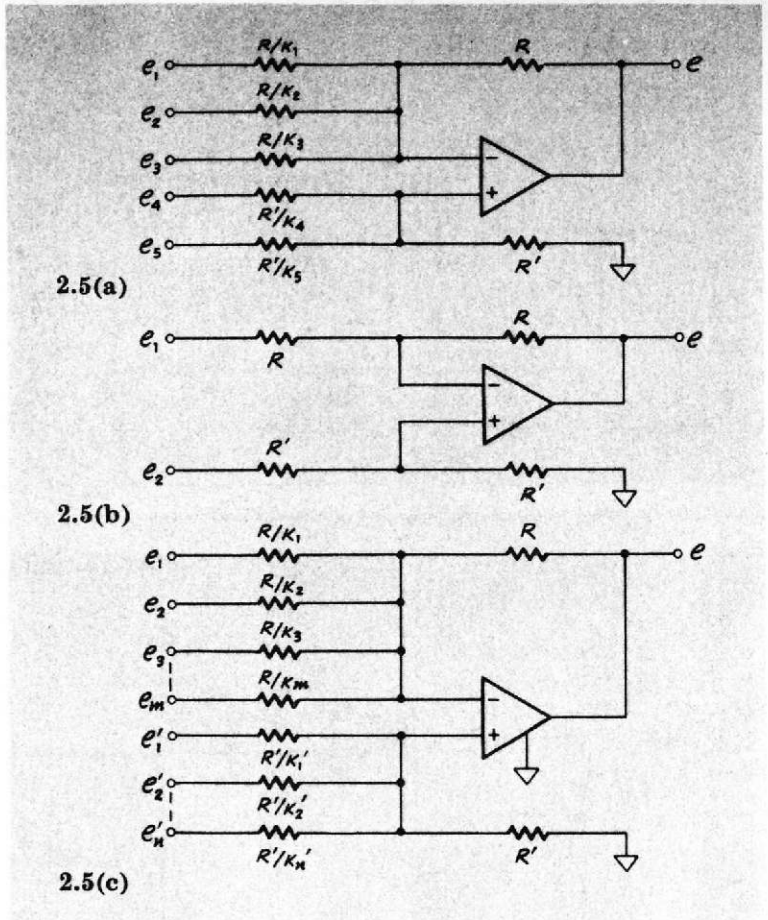
It should be noted that, in this as well as in the circuit of Figure 2.4, the input resistors indicated are each assumed to *include* the resistance of their voltage sources; indeed, this is always assumed in circuits in which an input resistor is shown connected to an ideal zero impedance source.

There is no theoretical restriction on the number of input paths that may be added to either side of this circuit. If there are "m" inputs to the negative-terminal summing point and "n" to positive-terminal summing point, as in figure (c), the general expression for response is:

$$e = \sum_{j=1}^{n} k_j' e_j' - \sum_{i=1}^{m} k_i e_i \qquad (2\text{-}13)$$

provided that:

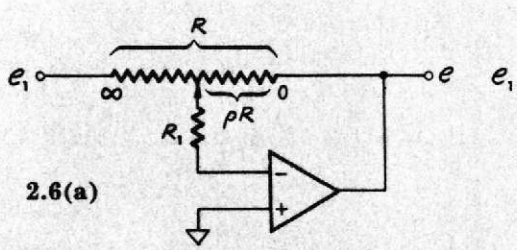
$$\sum_{j=1}^{n} k_j' = \sum_{i=1}^{m} k_i \qquad (2\text{-}14)$$

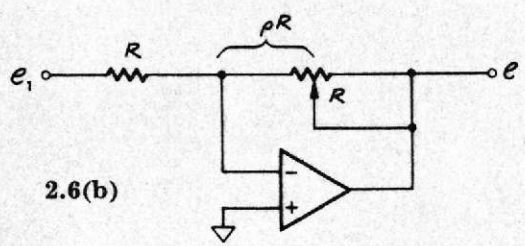


II.5
I.5
to
I.7
I.16
I.18
II.3
II.4
III.39
III.81

II.6 ADJUSTABLE-COEFFICIENT INVERTERS. In circuit (a) we have the true "adjustable electronic lever" with the tap of the potentiometer providing the adjustable "fulcrum." This results in a wide-range, variable-gain amplifier that may be precisely, if not conveniently, calibrated. A voltage gain of -1 occurs at mid-setting, while gains from a precise zero to very high values are within range. Note that a relatively small resistor, R_1, serves to protect the amplifier and prevent overload of the input source when ρ approaches unity. Note also that signal source impedance will generally affect the accuracy of the equation and limit the maximum gain.

If the potentiometer is placed in the feedback path alone, as in circuit (b), a proportioning device is obtained with narrower range than that of a circuit (a) but having a linear scale with respect to potentiometer rotation—a greater convenience, at times.





$$-e = \frac{\rho R}{(1-\rho)R} e_1 = \frac{\rho}{(1-\rho)} e_1 = \left(\frac{1}{\frac{1}{\rho} - 1}\right) e_1$$

$$-e = \frac{\rho R}{R} e_1 = \rho e_1$$

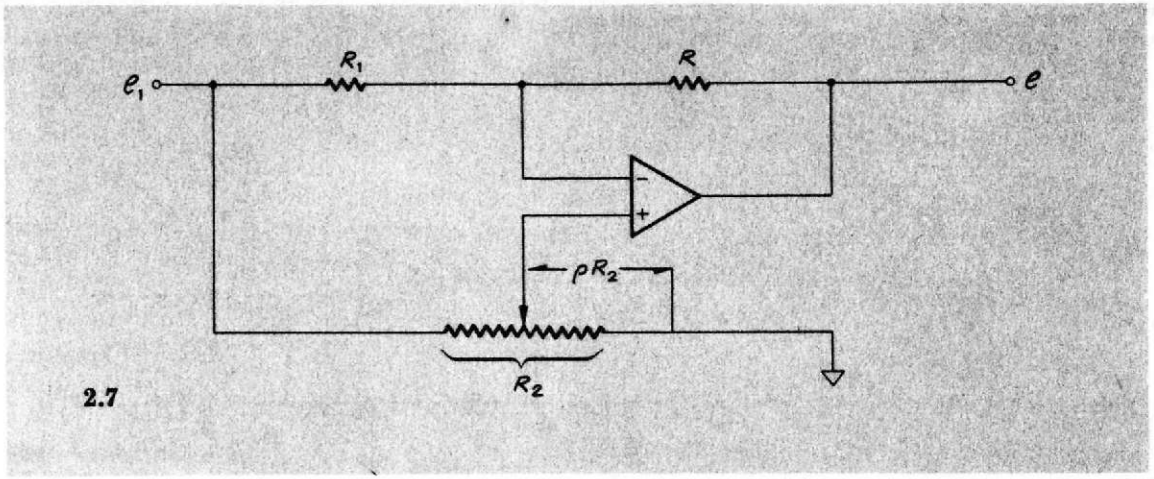
II.6
I.35
II.1
II.3
II.7
II.8

II.7 BIPOLAR ADJUSTABLE-COEFFICIENT CIRCUIT. It is but a short step from the end of II.6 to a circuit that draws upon the adder/subtractor technique to provide a wide and continuous range of coefficient adjustability, from a substantial negative value, through zero, to a substantial positive value. In the circuit shown, if $R = R_1$, the response varies between $+1$ and -1, linearly with rotation, passing through zero at $\rho = 0.5$. The relationship between ρ and the response is: (for $R = R_1$)

$$e = (2\rho - 1)e_1 \qquad (2\text{-}15)$$

Note that this useful circuit may be given a different upper-limit coefficient, by adjusting the ratio of R to R_1. The general expression for the response is:

$$e = \left[\left(1 + \frac{R}{R_1}\right)\rho - \frac{R}{R_1}\right]e_1 \qquad (2\text{-}16)$$



2.7

II.7
I.35
II.1
II.6
II.8
II.9

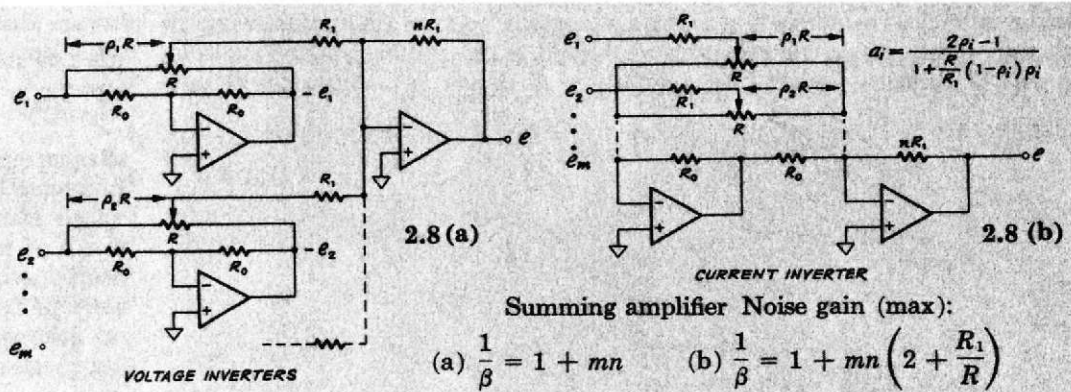
II.8 BIPOLAR ADJUSTABLE-SCALE COMBINOR. The circuits (a) and (b) perform identical mathematical operations.

$$e = n(a_1e_1 + a_2e_2 + \cdots a_me_m) \qquad (2\text{-}17)$$

Circuit (a) requires more amplifiers but these can be inexpensive types, since the circuit impedance level, R, is arbitrary.

Circuit (b) requires only two amplifiers. They are generally selected so as to have nearly equal performance, because their error contributions tend to be identical. Furthermore, the noise gain $(1/\beta)$ of the main amplifier of (b) is twice that of (a) if the current inverter is scaled so that it just avoids saturation (i.e., $R_0 = R_1/m$).

The noise gain of (b) is minimized by using large values of R, while (a) permits use of the lowest feasible values of R.



2.8 (a) 2.8 (b)

II.8
I.35
II.1
II.3
to
II.7
II.9

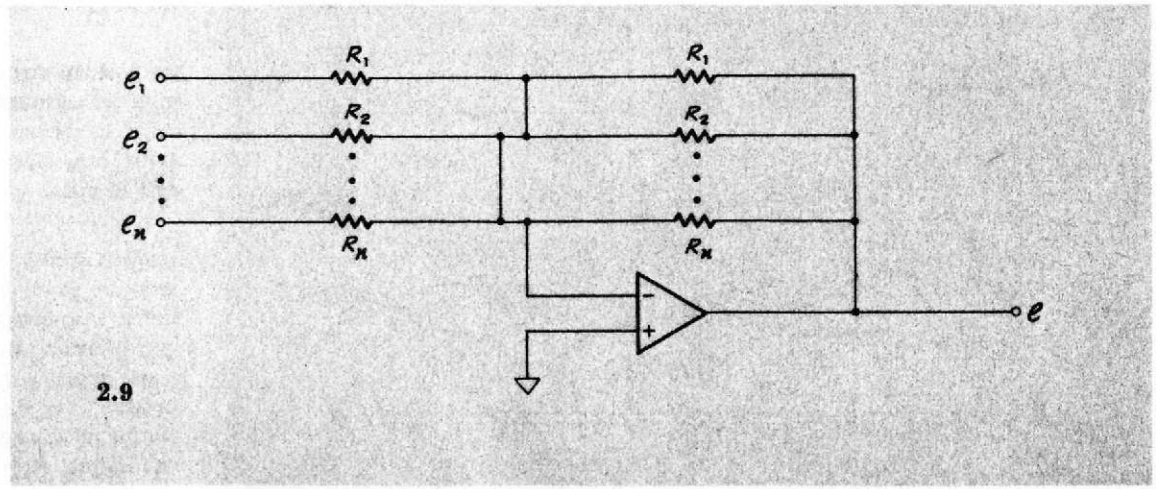
II.9 THE WEIGHTED AVERAGER. A special case of the Inverting Adder, or Linear Combinor (II.3), this circuit uses matching resistors in a voltage-dividing network that assures that the sum of the weighting coefficients is always precisely unity. The Weighted Averager yields an output that is the (inverted) weighted average of the inputs.

$$-e = a_1e_1 + a_2e_2 + \cdots + a_ne_n$$

where

$$a_k = \frac{1/R_k}{\frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_n}} \qquad (2\text{-}18)$$

and where $a_1 + a_2 + \cdots + a_n = 1$



2.9

II.9
II.1
II.3

II.10 SINGLE-INPUT AND SUMMING INTEGRATORS. The ability to integrate accurately is of fundamental importance in solving differential equations and modelling dynamic systems. The circuit of Figure (a) shows a simple running integrator (no reset or hold logic) that can be used within a stable feedback loop. In this circuit, in the ideal case, all the current flowing through the input resistor, e_1/R, must flow through the feedback capacitor. Hence:

$$-C\frac{de}{dt} = \frac{e_1}{R}$$

and thus

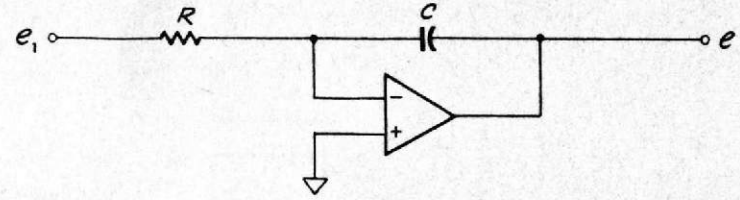
$$e = -\frac{1}{RC}\int^t e_1\,dt \qquad (2\text{-}19)$$

The *characteristic time* of the integrator is $T = RC$. (For example: $R = 1$ megohm, $C = 1\ \mu F$; $RC = 1$ sec.) This is the time required for the output to change by an amount equal to the average value of the input,

$$-\Delta e = \frac{\Delta t}{RC}\,\bar{e}_1 \qquad (2\text{-}20)$$

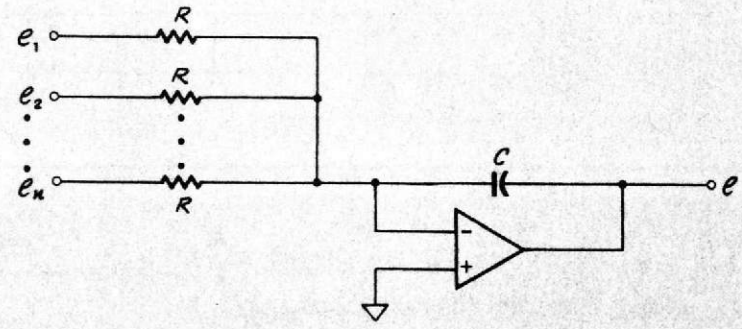
A very long characteristic time can be achieved by using a TEE network (I.26) of resistors in place of the input resistor, and a large, low-leakage feedback capacitor. For example, a 10 μF polystyrene capacitor, together with an effective 100 megohm TEE network, gives a 1000-second (16⅔ min.) characteristic time. In this example, the amplifier offset current must be low, since even 10 pA of offset produces an error equivalent to that caused by 1 mV of voltage offset. On the other hand, the capacitor leakage resistance may become the dominant error factor, since it must exceed 10^{12} ohms, at 10 volts of output, for the leakage current to be less than 10 pA.

For high-speed operation, a 1 m sec. time constant ($R = 10$ kΩ, $C = 0.1\ \mu$F) may be taken as typical. In this case, leakage current is not of great concern unless there is to be a long "hold." (See II.12, III.57.)



2.10(a)

$$-e = \frac{1}{T}\int^t e_1\,dt \equiv \frac{1}{Tp}\,e_1$$



$$-e = \frac{1}{T}\int^t (e_1 + e_2 + e_3 + \cdots + e_n)\,dt$$

2.10(b)

$$T = RC$$

Adding more inputs to achieve a summing integrator is illustrated in (b). By choosing unequal input-resistor values, the contributions to the output (integral) of the several inputs may be weighted, in direct proportion to their conductance.

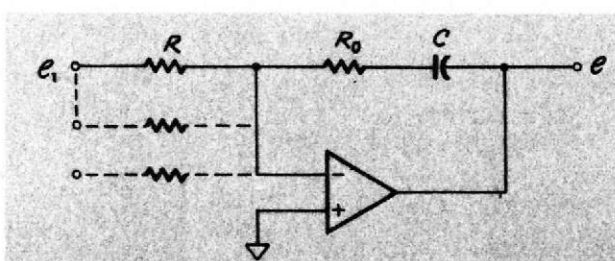
II.11 THE AUGMENTING INTEGRATOR. When a resistance, R_0, is placed in series with the feedback capacitor of an integrator, the circuit will produce a composite output, containing a component proportional to the input signal, added to a component proportional to the *time-integral* of the input signal.

This circuit has applications in closed-loop controllers (to provide a proportional-plus-reset control action) as well as in the simulation of many commonly-encountered physical systems. It is adaptable to summing and differential integrators, too, with and without weighting. By adding R_0 in series with C in 2.10 (b), for example, we create a response given by:

$$-e = \frac{R_0}{R}\left(1 + \frac{1}{Tp}\right)(e_1 + e_2 + \cdots + e_n) \qquad (2\text{-}21)$$

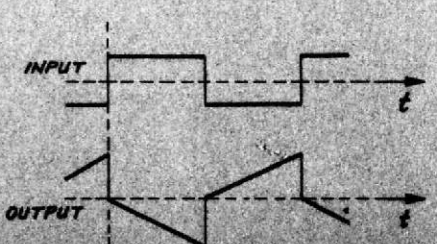
where

$$T = R_0C$$



$$-e = \frac{R_0}{R}\left(1 + \frac{1}{R_0Cp}\right)e_1$$

2.11(a)



2.11(b)

II.12 PRACTICAL CONSIDERATIONS IN INTEGRATOR DESIGN.

The free-running-integrator circuit of II.10 must be used within a stable feedback loop, because it contains no inherent provisions for forcing it to an arbitrary output (initial) condition at an arbitrary time (time zero) . . . and an open-loop free-running integrator will, in time, drift to one of its bounds.

The most common way to impose an arbitrary initial condition upon an open-loop integrator is to use a relay circuit, such as (a). (See also II.49, II.50, and II.51.) Externally-generated logic signals are then used to control the mode—*run*, *set*, or *hold*. Figure (b) shows a typical output history. During each *set* mode interval, the integrator output relaxes to $E_{I.C.}$ in accordance with:

$$e = E_{I.C.} + (e_s - E_{I.C.})\epsilon^{-\frac{t}{R_B C}} \qquad (2\text{-}22)$$

where e_s is the value of e at the start of the *set* interval. The *set* interval must last long enough to allow the transient to subside ($7R_BC$, for 0.1% accuracy). For fast reset, R_B should be very low.*

If current through R_A must be avoided, one may use two amplifiers, resetting the integrator to a zero initial condition (R_A "infinite"), and then, as shown in (c), adding the arbitrary initial condition in a separate summing amplifier. Note that in (c), because R_B is very small, one cannot ground the back contact of the *set* relay, as is done in (a), to minimize relay leakage current during the *run* and *hold* modes. In (c), one can attenuate in A and amplify in B, scaling the circuits so as to impose any arbitrary full-scale initial condition (within the ratings of B) without saturating A.

When switching from *set* to *run*, it is necessary to avoid having both relays of circuit (a) closed at the same time, lest an error (indicated by dashed lines at the right of the history graph), be introduced. This error can be avoided by going through an intermediate *hold* state, also indicated in Figure (b), possibly at the expense of control-logic simplicity. (The *hold* state is a logical *requirement* in some systems, anyway.)

When several integrators are involved in a simulation, errors may be introduced if they do not all switch modes simultaneously. These errors are small if the characteristic time is large compared to relay-closure time differences.

In the *hold* mode, the output will tend to drift at a rate $\bar{I}C$, where $\bar{I}$ represents the average sum of all unwanted currents.

Hence, it would appear that the larger the capacitance (for a given total leakage current) the better. However, practical capacitors have a leakage conductance directly proportional to capacitance. When great care has been taken to minimize all *other* sources of leakage, such as amplifier input current and relay insulation, no substantial improvement in drift rate is possible by using a high quality (polystyrene) capacitor greater than 1 μF.

In the *run* mode, another source of drift appears. The amplifier offset voltage drives, through the sum of all input admittances, an additional error current. Thus, for minimum drift in the *run* mode, an amplifier with both low offset current *and* low offset voltage is required. In the *hold* mode, as noted, only offset *current* must be minimized, assuming that the amplifier's input resistance is sufficiently high to minimize the error current due to voltage offset.

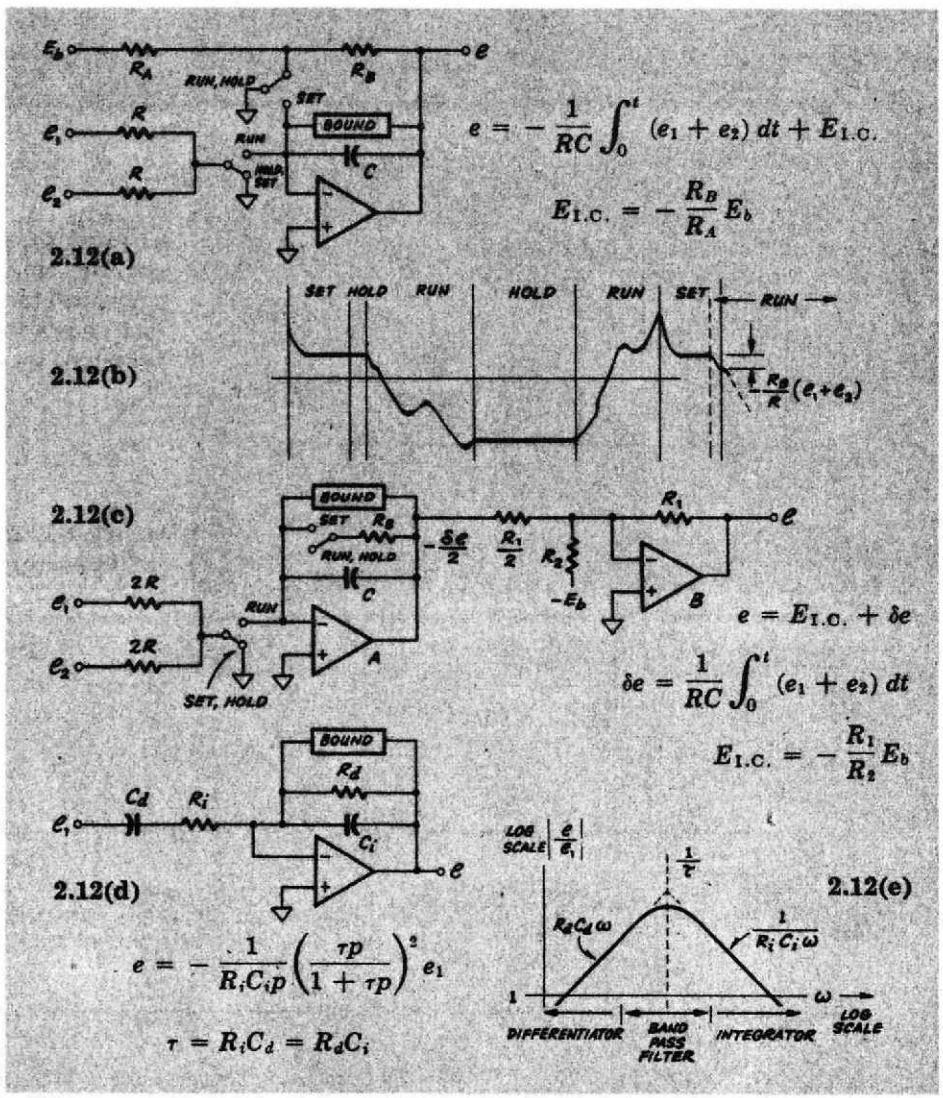
*To protect the relay contacts, R_B must be at least 10–100 Ω.

If there is a possibility that the amplifier output voltage range may be exceeded, a feedback-circuit bound is desirable. This enables the integrator to respond immediately if the net input changes sign. By properly guarding the bound (see I.25) leakage can be made less than 10^{-12}A.

Instead of relay resetting, AC coupling, as in (d), can be used to prevent integrator runaway. (See also III.73.) Depending upon the frequency range of interest, this circuit can serve as a differentiator (at low frequencies), a band-pass filter (at mid-frequencies), or an integrator at high frequencies. Then,

$$e = -\frac{1}{R_iC_ip}\left(\frac{R_iC_dp}{1+R_iC_dp}\right)\left(\frac{R_dC_ip}{1+R_dC_ip}\right)e_1 \qquad (2\text{-}23)$$

Usually, $R_iC_d = R_dC_i$, see also III.73.



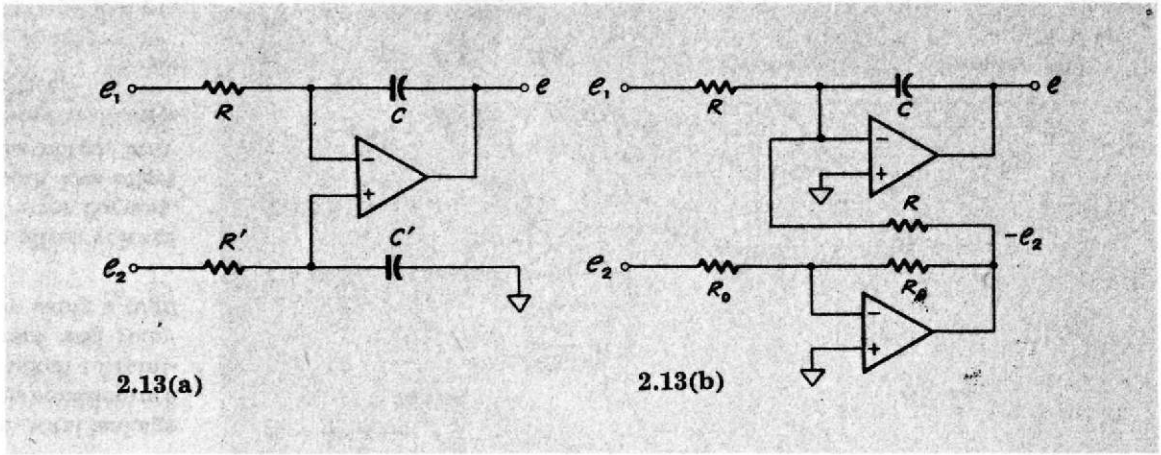
II.12
I.6
I.7
I.11
I.12
I.13
I.14
I.18
I.25
I.33
I.36
II.10
II.11
II.13
II.14
II.21
II.49
II.50
II.51
III.27
III.46
III.57
III.73

II.13 THE DIFFERENCE INTEGRATOR. Having gone this far, it takes little daring, we submit, to replace two of the resistors in the adder-subtractor of II.5 with capacitors, thus creating the circuit shown here, in which the output is, at every moment, proportional to the time-integral of the difference between two signals

If $RC = R'C'$, the input-output relationship is simplest:

$$e = \frac{1}{T}\int^{t} (e_2 - e_1)\, dt \qquad (2\text{-}24)$$

Because two capacitors are used, the set-run-hold problems outlined in II.12 are compounded in the differential circuit of (a). Hence, circuit (a) is happiest in applications in which the loop is closed externally. Please note that an inverter and a summing integrator will do a similar job, as shown in (b).



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II.12
III.12

II.14 DOUBLE INTEGRATOR. This extension of the basic integrator of II.10 permits a single amplifier to generate the second time-integral of an input signal. It is sometimes useful in handling dynamic system equations such as:

$$\frac{d^2x}{dt^2} + ax = f(t) \qquad (2\text{-}25)$$

The response of this circuit is given by:

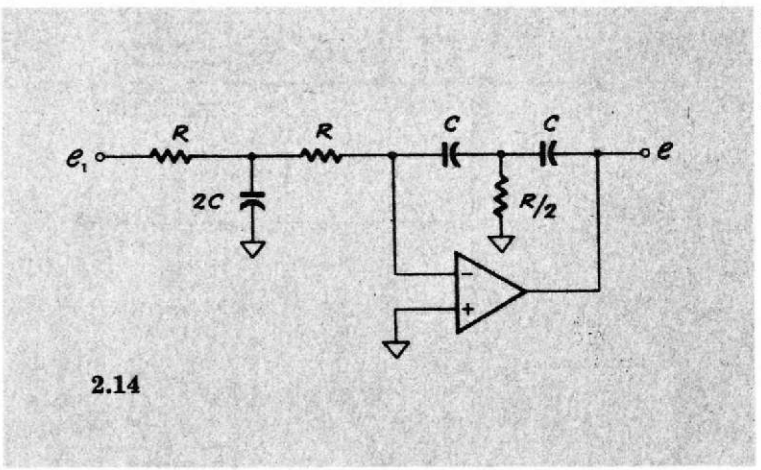
$$-e = \frac{1}{R^2C^2p^2}e_1 = \frac{1}{(Tp)^2}e_1 \qquad (2\text{-}26)$$

where $T = RC$

If the output is connected back to the input, this circuit will oscillate at a frequency given by:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi T} \qquad (2\text{-}27)$$

When this circuit is connected as an oscillator, it is desirable, in practice, to modify the time-constants so that the feedback time constant is slightly shorter, and the input time constant is correspondingly longer, ensuring regenerative damping and (hence) buildup.



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III.10

II.15 SIMPLE LAG. After a delay equal to many time constants ($t \gg RC$) this circuit, in response to a "step" input at e_1, settles down to behave like any other arbitrary-coefficient inverter, approaching the familiar response of:

$$e = -\left(\frac{R}{R_1}\right)e_1 \qquad (2\text{-}28)$$

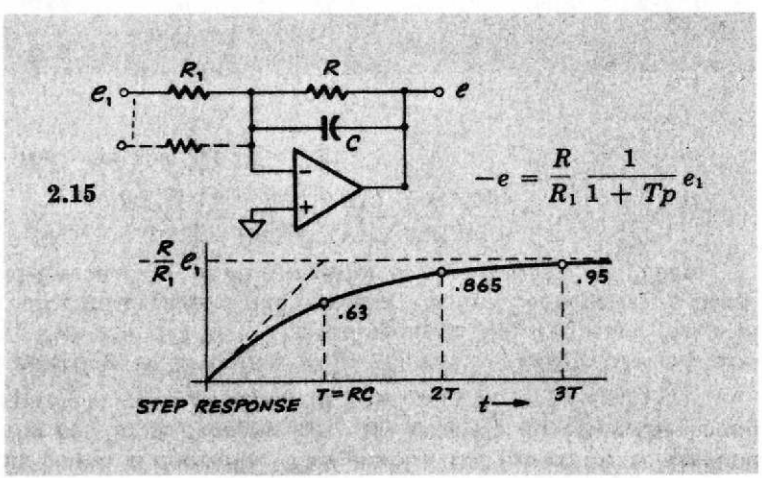
Initially, however, it behaves like an integrator, and then its output exponentially approaches the inverter response at steady state. The net effect is to *delay* the appearance of the above-stated response . . . it "lags" the appearance of the input. This is called performing a "tardigrade" operation on $e_1(t)$. e_1 need not be a step function, of course; regardless of the variation of e_1 with time, the generalized response equation is:

$$-\frac{R}{R_1}e_1 = (1 + Tp)e \qquad (2\text{-}29)$$

in operational notation, in which

$$pe \equiv \frac{de}{dt} \quad \text{and} \quad T = RC$$

Note that changing R affects both gain (R/R_1) *and* time-constant (T); while changing R_1 affects only the gain. Note also that the lag may be applied to the *sum* of several inputs, as indicated in dashed lines, and weighting may be accomplished, also, by proportioning the input resistors.



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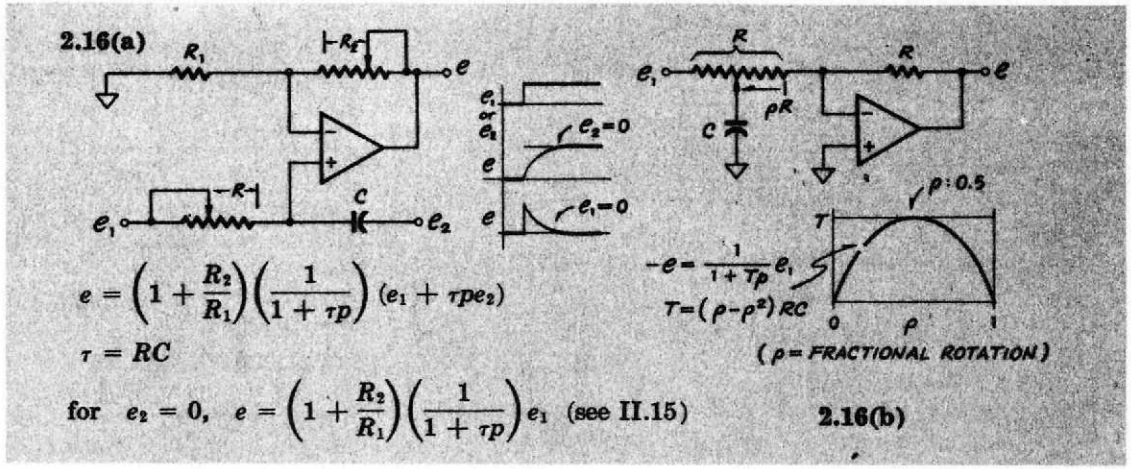
II.16
III.54

II.16 ADJUSTABLE-LAG CIRCUITS. These two circuits permit continuous manual adjustment of the lag-response time constant, over a wide range. Circuit (a) provides independent adjustments of time constant and gain. The amplifier should have high *CMRR*; for long time constants, it must also have low input offset current. By driving the e_2 input, a high-pass filter characteristic (imperfect differentiator) can be realized. Both e_1 and e_2 must be driven from low impedance (or grounded.)

Circuit (b) is useful when inverting amplifiers must be employed, perhaps to gain the advantages of chopper stabilization; however, one must overcome the following drawbacks and inconveniences: dynamic instability at extreme settings; the general unavailability of high-resistance potentiometers; need for matching the feedback resistor to the potentiometer resistance.



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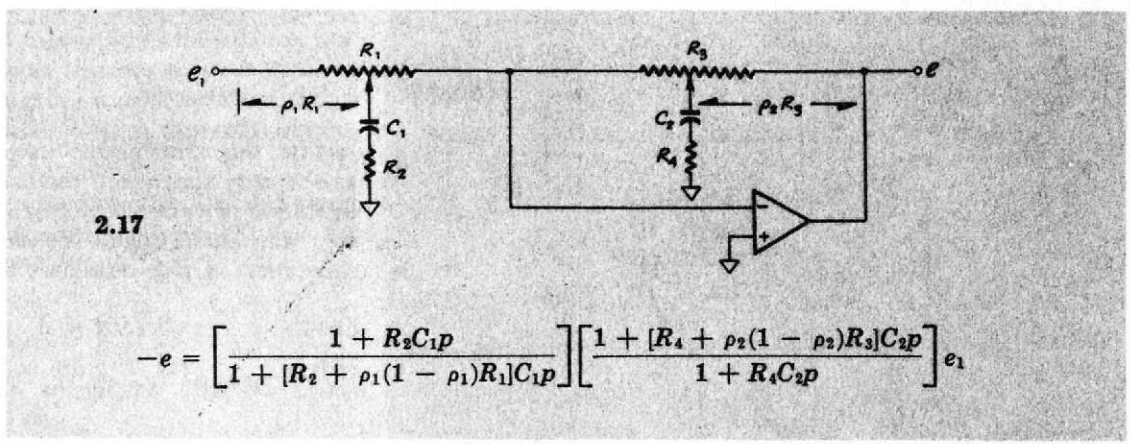
III.23
III.26

II.17 LAG-LEAD ELEMENT. Introducing a lag into the feedback circuit (as well as into the input circuit, as was done in the preceding section) creates the possibility of a leading response, if the time constant in the feedback circuit is the greater of the two. If, as shown, we make both time-constants adjustable, we may arbitrarily change the response of the circuit from leading to lagging, merely by adjusting the time constants, relative to each other. When the time-constants are equal, the circuit becomes a unity-gain inverter. R_2 and R_4 insure dynamic stability.

This example illustrates a fairly general, yet flexible, configuration typical of many used for "lag-lead" compensation in instruments and controllers, and in the representation of thermal systems.



II.17
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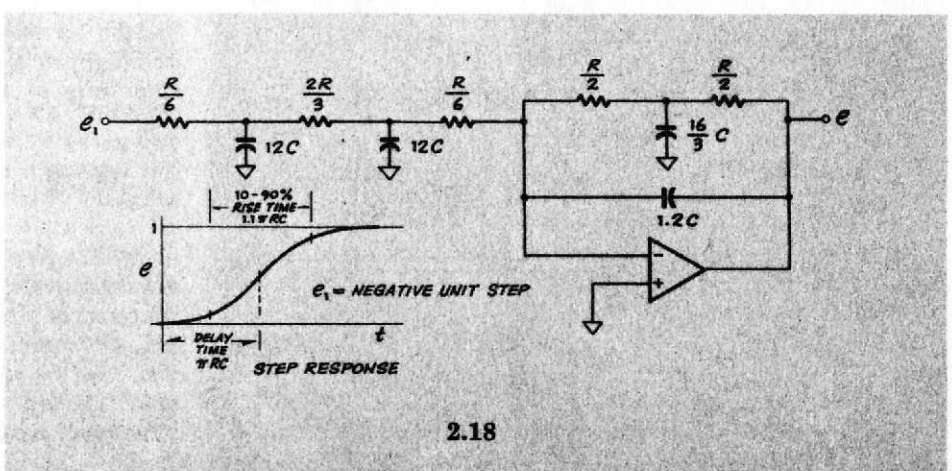
II.16

II.18 DELAY-LINE ELEMENT. This circuit is a third-order low-pass filter having phase lag nearly linear with frequency ($\phi \alpha \pi\omega RC$) in the range from 0 to 180°. In this sense, it approximates a delay, exp $(-\pi RCp)$, although, unlike a pure delay, amplitude rolls off considerably $\left(\left|\frac{e}{e_1}\right|_{\phi = 180°} = \frac{1}{3}\right)$. Amongst the merits of the circuit we may list the following: its transient-step response has no overshoot; its delay-time-to-rise-time ratio is nearly unity; and its first two derivatives are zero at zero time. The transfer operator is:

$$e = -\frac{1}{(1 + 2RCp)(1 + 1.2RCp + 1.6R^2C^2p^2)}e_1 \qquad (2\text{-}30)$$

Note that there is a finite time delay before any appreciable response occurs, following which the response exhibits a rise time of the same order of magnitude as the delay. To improve the ratio of delay time to rise time, a number of stages (n) may be cascaded; the ratio increases as $\sqrt{n}$.



II.18
III.23
III.24

II.19 DIFFERENTIATOR. Circuit (a) is of an "ideal" differentiator. The current into the summing point through C is:

$$i_c = C\frac{de_1}{dt} \qquad (2\text{-}31)$$

and the feedback current, through R, must, in the ideal case, equal i_c, so that:

$$-e = i_c R = RC\frac{de_1}{dt} = Tpe_1 \qquad (2\text{-}32)$$

where $T = RC$ and $pe_1 = \frac{de_1}{dt}$

As we well know from earlier disillusionment, circuit (a) will not be dependably stable without at least a small feedback capacitor, like C_r. C_r is a good idea for at least one other reason: circuit (a) has a nasty preference (i.e., gain) for high-frequency noise, which tendency is much ameliorated by a gentle but firm roll-off above useful frequencies. Now, however, we no longer have a true differentiator; C_r has changed that.) (See II.21 for design consideration.)

Figure (b) shows that we may combine the derivatives of several signals in one Summing Differentiator. By now, this comes as no surprise to any student of the fearful symmetry of nature—after all, we have already seen adders and summing integrators . . . why not summing differentiators? As might be expected, weighting of the individual derivatives is entirely practical, merely by proportioning the input capacitors. The ideal response equation for n inputs is:

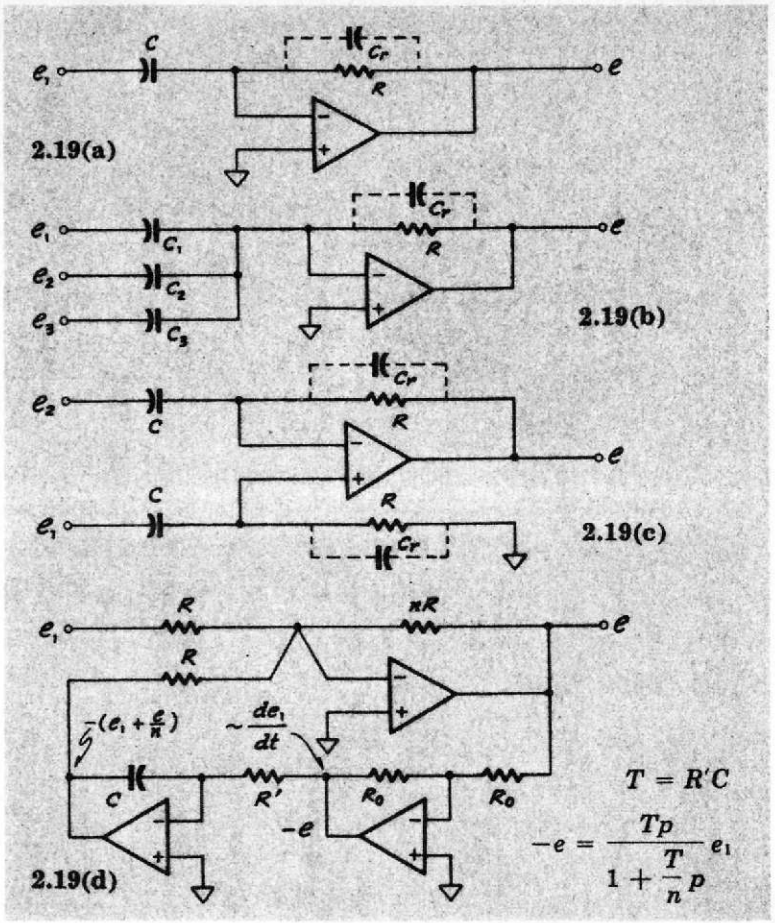
$$-e = RC_1pe_1 + RC_2pe_2 + \cdots RC_npe_n \qquad (2\text{-}33)$$

Figure (c) supports the theory of Harmony Throughout The Universe. It is a difference differentiator—that is, it produces an output proportional to the difference between two derivatives. For equal time-constants, the output expression is:

$$e = Tp(e_1 - e_2) \qquad (2\text{-}34)$$

where $T = RC$

Figure (d) shows a scheme that is commonly used in general-purpose analog computors. To maintain dynamic stability, one must not make n too large. In general, stabilizing this loop is more difficult than stabilizing the single-amplifier circuit 2.21 (b).

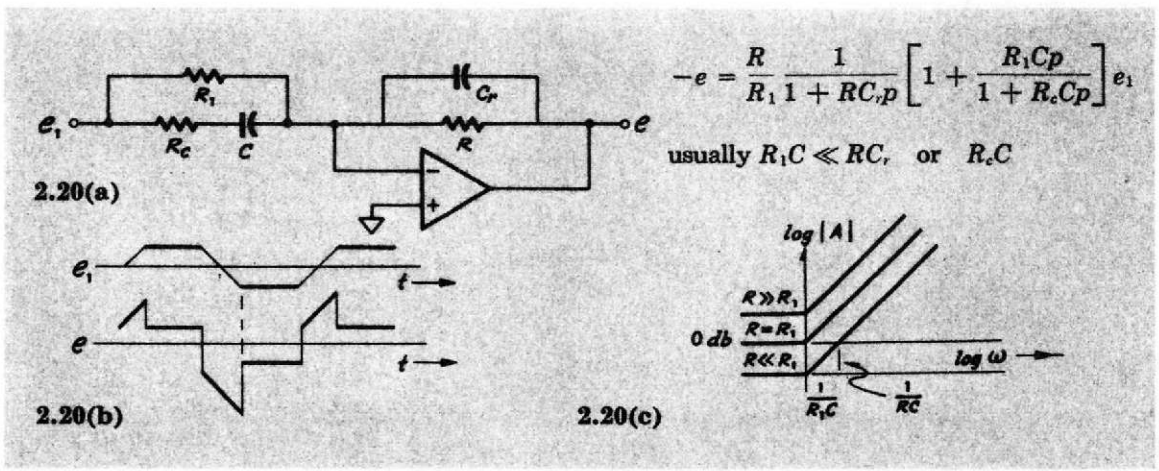


II.20 THE AUGMENTING DIFFERENTIATOR. The response of circuit (a) may be found by simple superposition, since the current contributions of R_1 and C are independent because of the amplifier's summing property. The output voltage must furnish both currents, mainly through R, except at high frequencies above the useful differentiating bandwidth. The ideal response is given, therefore, to a good accuracy, by:

$$-e = \frac{R}{R_1}(1 + Tp)e_1 \qquad (2\text{-}35)$$

where $T = R_1C$

and is illustrated in the exemplary graph of (b). The frequency response of this circuit is given in (c).



II.21 PRACTICAL CONSIDERATIONS IN DIFFERENTIATOR DESIGN. In II.19 we mentioned the need for a small feedback capacitor to limit the gain at high frequencies and to provide dynamic stability. A further modification of the "ideal" differentiator circuit involves placing a small resistor in series with the input capacitor. This resistor also helps to limit the high frequency gain, and to ensure dynamic stability; furthermore it "cushions" the signal source by reducing the effective magnitude of the capacitive load seen at the input, and it limits the maximum input current. The addition of this resistor makes the practical differentiator circuit of (b) identical in form to the AC integrator circuit, Figure 2.12(d).

Circuit (b) is dynamically unstable (or at best marginally stable) if either R_i or C_i is absent, or if either is not high enough in value. To achieve well damped stability, the radian frequency, $\omega_c (=1/\tau_c)$ should be chosen to be no greater than the geometric mean between $\frac{1}{R_dC_d}$ and the amplifier's gain-bandwidth product, ω_H. (See I.43.)

$$\tau_c > \sqrt{\frac{R_dC_d}{\omega_H}} \quad \text{or} \quad R_iC_i > \frac{1}{\omega_H} \qquad (2\text{-}36)$$

Wisdom often dictates choosing a substantially *larger* value of τ_c (than the geometric mean) in order to limit the sensitivity of the differentiator to high-frequency noise.

The differentiator characteristic time, R_dC_d, is selected so that the maximum rate of change of input signal will produce full-scale output. I.e., set

$$R_dC_d = \frac{|e|_{\max}\ (\text{f.s.})}{\left|\frac{de_1}{dt}\right|_{\max}} \qquad (2\text{-}37)$$

Occasionally, a still faster (i.e., off-scale) input change may occur. The bound circuit shown in (b) will limit the output in that event, and prevent an erroneous charge from developing across C_d. Thus protected from off-scale saturation, the output will respond correctly, even immediately following an anomalous steep transient.

For moderately-fast signals, choose R_d so that full-scale voltage across R_d develops between 0.1 and 1 milliampere in it; however, if this computation calls for a (polystyrene) capacitor for C_d higher than 1 to 10 μF, it is better (because of capacitor leakage) to limit the capacitor value to 10 μF, and permit larger values of R_d in order to achieve a long enough characteristic time. In such a design, the full scale signal current will thereby be reduced, necessitating the selection of an amplifier with a correspondingly lower offset current rating, for accuracy, and higher input impedance, too. An exotic example of this procedure is given in III.56, which describes a differentiator design having a 10^6 second (nearly 2-week!) characteristic time.

The effective error produced by DC summing-point voltage and current offsets (E_0 and I_0) referred to the input is:

$$\left(\frac{de_1}{dt}\right)_{\text{error}} = \frac{1}{C_d}\left[\left(\frac{1}{R_d} + \frac{1}{R_{in}}\right)E_0 + I_0\right] \qquad (2\text{-}38)$$

where R_{in} is the amplifier's effective input resistance.

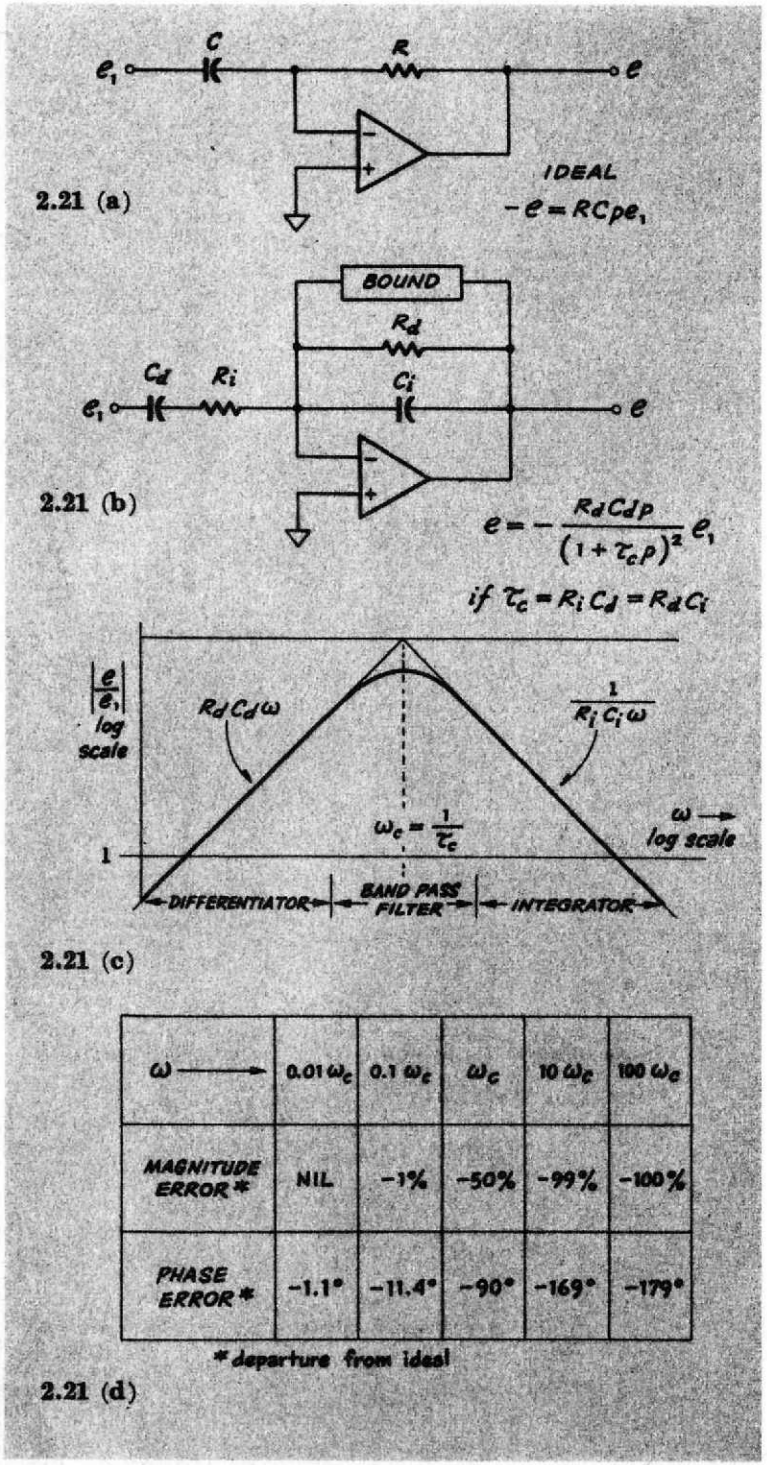
Choose the "critical" radian frequency:

$$\omega_c = \frac{1}{\tau_c} = \frac{1}{R_iC_d} = \frac{1}{R_dC_i} \qquad (2\text{-}39)$$

as low as possible without causing excessive distortion (i.e., gain and phase error). The table (d) may prove helpful in assessing the gain and phase errors caused by the two lagging time constants R_iC_d and R_dC_i. Note that by substituting $j\omega$ for the operator p in the input-output relation the gain and phase are given by:

$$-\left|\frac{e}{e_1}\right| = \frac{R_dC_d\,\omega}{1 + \tau_c^2\omega^2} \qquad (2\text{-}40)$$

$$\phi_{\text{lead}} = 90° - 2\tan^{-1}\tau_c\omega \qquad (2\text{-}41)$$



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III.56

II.22 INHERENTLY NON-LINEAR ELEMENTS. We have already seen (in I.32—DIODES) that certain semiconductor junctions exhibit a reasonably-accurate logarithmic relationship between voltage and current, over quite wide ranges of current. This *inherent* non-linearity is so useful, that many years have been devoted to the refinement of inherently logarithmic devices — searching out those that adhere with the greatest fidelity to the formula:

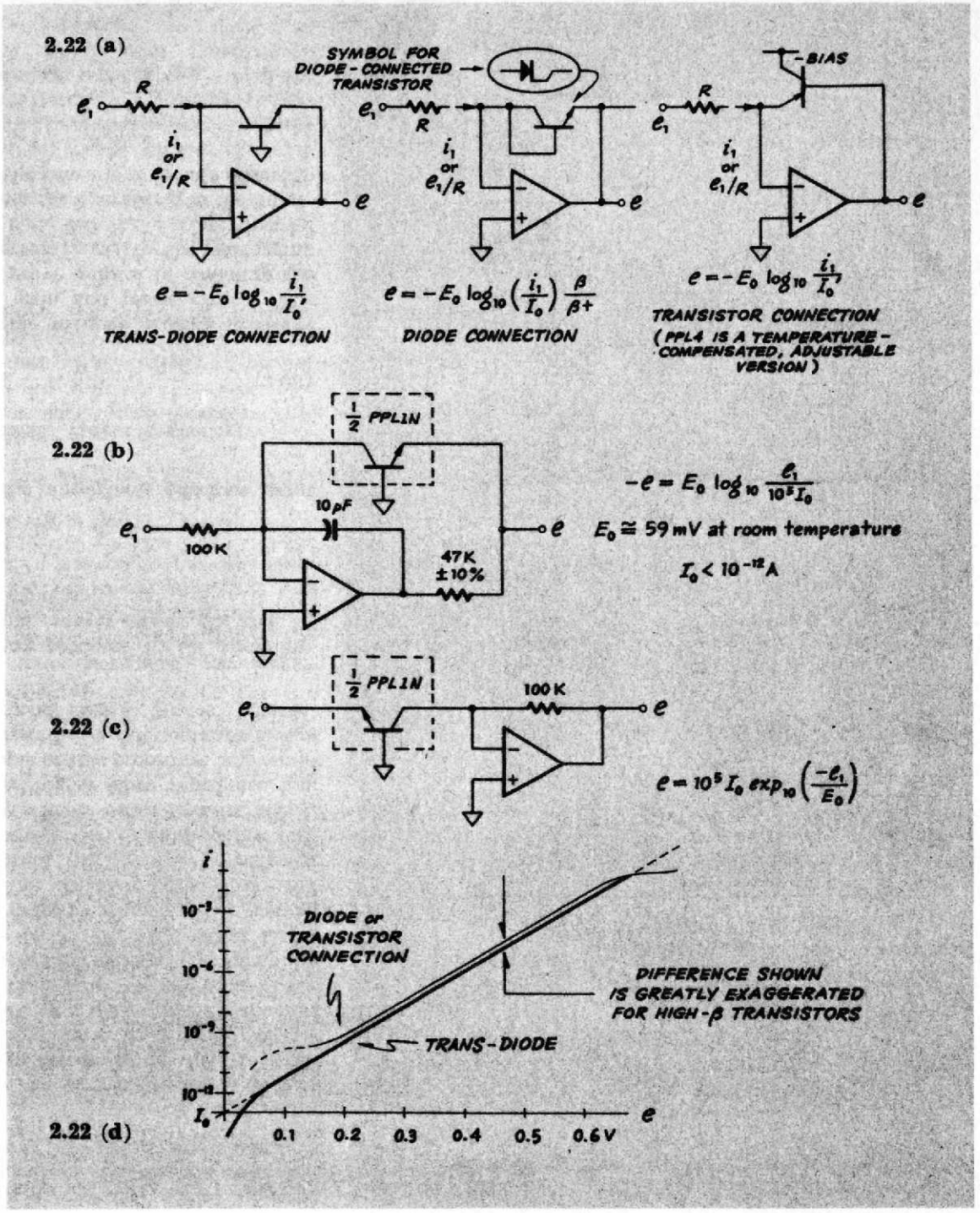
$$e = E_0 \log_{10}\left(\frac{i}{I_0}\right) \qquad (2\text{-}42)$$

over the widest possible ranges of i, and then domesticating them . . . by such means as temperature compensation, matching pairs, etc. These efforts have been crowned at Philbrick by the development of a family of devices known as LOGARITHMIC TRANSCONDUCTORS. The configurational versatility of typical members of this family is summarized briefly in Figure (a). Circuits (b) and (c) show the application (without temperature compensation) of just one form of these Transconductors to the generation of elementary log and anti-log functions. (See II.28–31 for fuller exposition.) The graph of Figure (d) shows the ranges over which the PL1/PPL1 transconductors adhere closely to the straight and narrow path.

Back in the dim past, it was not uncommon to use the more-or-less-square-law behavior of a vacuum-tube triode transfer characteristic to achieve quadratic nonlinearity; and the uses of nonlinear effects in vacuum tubes, transistors, capacitors, varistors, etc., still appear from time to time as preferred solutions to specific problems, in which compromises among functional fidelity, temperature sensitivity, and bandwidth are acceptable.

Specific recent examples include the multiplicative properties of field-effect transistors, and the clever use of silicon carbide for squaring in the Douglas Quadratron (now available from Bourns, Inc.).

Finally, no summary of inherently nonlinear elements for functional representation, however brief, would be complete without mention of the Hall effect. If any conductor carrying a current is placed in a transverse magnetic field, a voltage proportional to their true cross-product will appear across the conductor along the third axis. The constant of proportionality known as the *Hall Coefficient*, extremely small for most conductors, is appreciable in some recent devices. However, Hall-effect multipliers suffer from asymmetry and lack of common scaling, and they tend to be temperature-sensitive, but for many applications they are quite useful. Operational Amplifiers are used with Hall-effect devices for scaling, as current sources, and for field-driving.



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III.68

II.23 SYNTHESIZED-FUNCTION NON-LINEAR ELEMENTS. Another fundamental way to create a known and dependably-reproducible nonlinear device is to construct a network, the elements of which are not in themselves selected for inherently-conformal nonlinear behavior, but which, when combined and proportioned appropriately, exhibit the desired nonlinear e/i relationship. Although such synthetic networks are invariably more ramified than are the inherently nonlinear devices, particularly if they must be very accurate, they offer far greater design freedom in the range and variety of available nonlinear functions. Time and toil have brought forth gratifyingly-accurate networks that exhibit logarithmic, transcendental, and quadratic behavior, and accommodate various combinations of voltage and current polarity. In their most convenient form, they appear as a family of Philbrick Operational Plugins, described briefly on the inside back cover of this manual, under the designations: PSQ-N/P, SPLOG-N/P, SPSIN-N/P, SPCOS-N/P, and SPFX-N/P. For the ultimate in flexibility, we commend to you the SK5-F.* Circuit (a) is a simplified generic schematic of such a network. The graphical analysis (b) that accompanies it shows how such a network can be made to conform—at least grossly—to a particular arbitrary function. The input signal, e_1, is connected to n networks, each forming a divider between e_1 and a negative reference voltage, E. Above some value of e_1, the diode will conduct, driving a current into the summing point. The necessary condition for diode conduction in the first branch is:

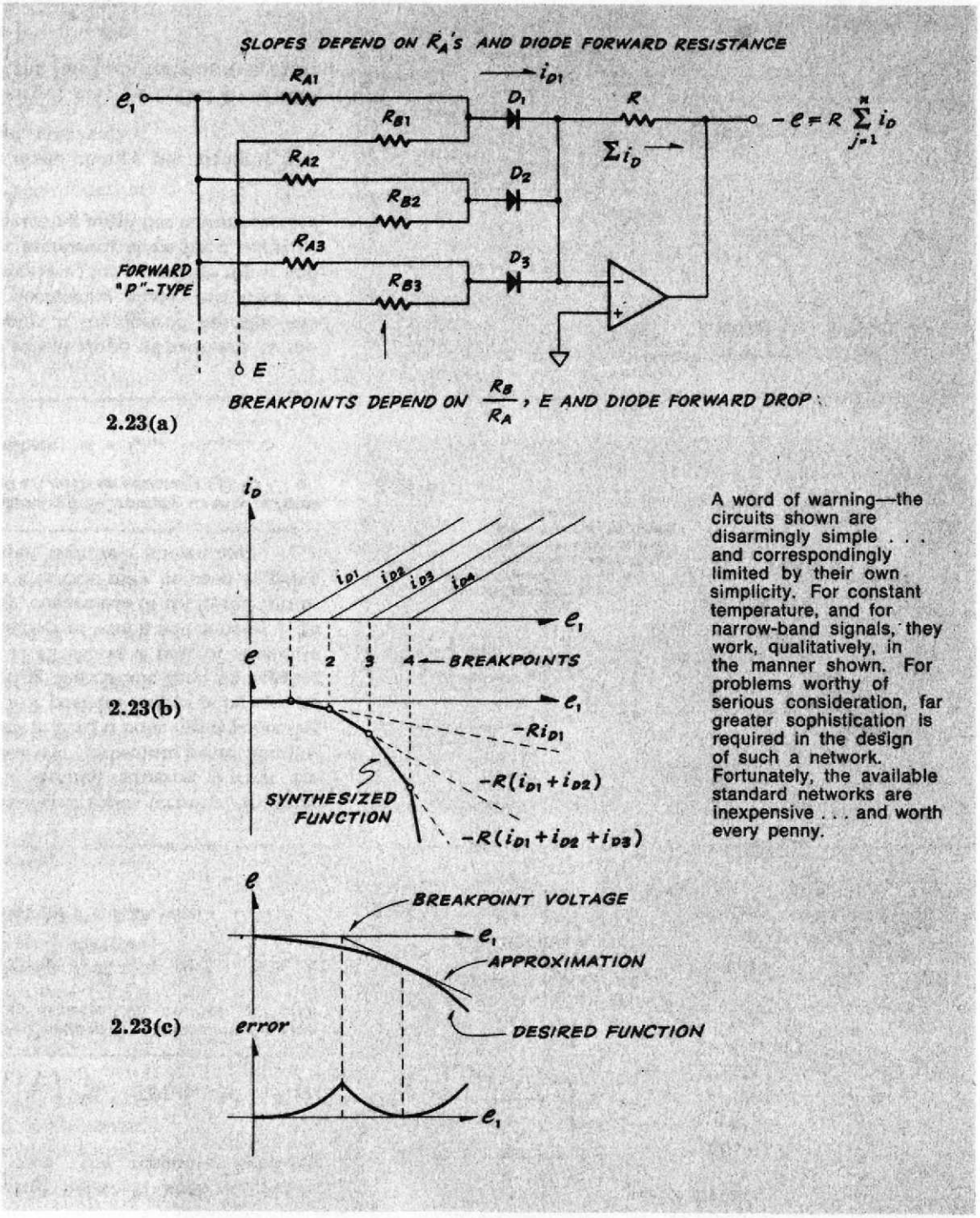
$$e_1 \geqq \frac{R_{A1}}{R_{B1}} E \qquad (2\text{-}43)$$

above which, the current that flows to the summing point (neglecting diode drop) is e_1/R_{A1}, since feedback from the amplifier (through R) holds the summing point at a virtual ground (zero) potential. The complete expression for the current in D_1, then, is: (for $i_{D1} > 0$)

$$i_{D1} = \frac{\left(e_1 - \frac{R_{A1}}{R_{B1}} E\right)}{R_{A1}} = \left(\frac{e_1}{R_{A1}} - \frac{E}{R_{B1}}\right) \qquad (2\text{-}44)$$

The difference between the desired function and the synthesized approximation is the systematic error of the device. Figure (c) shows such an error for an approximation made by line segments tangent to the desired function. Usually, these errors are expressed in percentage of full scale output. Use additional diodes (and associated reference voltages) connected in opposite polarity, and/or additional amplifiers, to invert input voltages or computing currents if input voltages of opposite polarity are to be dealt with or non-monotonic functions to be embodied.

*The SK5-F Manual should interest those who find this treatment of arbitrary nonlinearity intolerably brief.



A word of warning—the circuits shown are disarmingly simple . . . and correspondingly limited by their own simplicity. For constant temperature, and for narrow-band signals, they work, qualitatively, in the manner shown. For problems worthy of serious consideration, far greater sophistication is required in the design of such a network. Fortunately, the available standard networks are inexpensive . . . and worth every penny.

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II.24 BASIC CIRCUIT—LOG OR ROOT RESPONSE.

If we connect a nonlinear network (see 2.23(a)) so that the network is driven by the amplifier output and feeds back a current related to the voltage in a predictably-nonlinear manner, the response of the circuit will be:

$$e = -f^{-1}\left(\frac{e_{in}}{R}\right) \qquad (2\text{-}45)$$

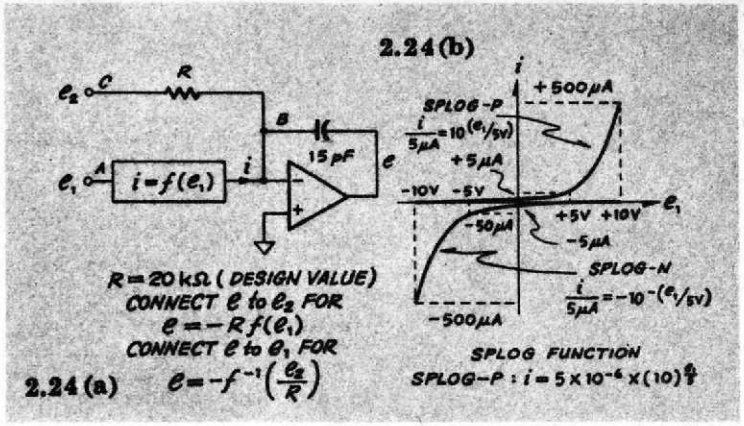
where f is the causal functional relationship between the voltage at A and the current into B. This circuit may be used to develop inverse functions. If, for example, we used Model PSQ-N (square-law characteristic), the response of the circuit connected for the inverse function (i.e., square root) would be:

$$-e = \sqrt{10e_{in}} \quad \text{for} \quad R = 20\ \text{k}\Omega \qquad (2\text{-}46)$$

If an exponential network, such as Model SPLOG*, is used, the response becomes: $(e_2 < 0)$

$$e = \log_{10}\left(-\frac{e_2}{0.1\ \text{V}}\right) \quad \text{for SPLOG-P} \qquad (2\text{-}47)$$

*SPLOG-P/N are designed to operate over a current range of four decades (.05 to 500 μA) with an error (@ 25°C) of: $\left|\frac{\delta i}{i_{\text{desired}}}\right| < .01$ for $i > 5\ \mu$A and $\left|\frac{\delta i}{i_{\text{max}}}\right| < .0001$ for $i < 5\ \mu$A where $\delta i = |i_{\text{actual}} - i_{\text{desired}}|$.



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II.25 SQUARER.

Here we show a form of circuit 2.23(a), in which the nonlinear network is a PSQ-P Quadratic Transconductor, which has the basic e/i relationship:*

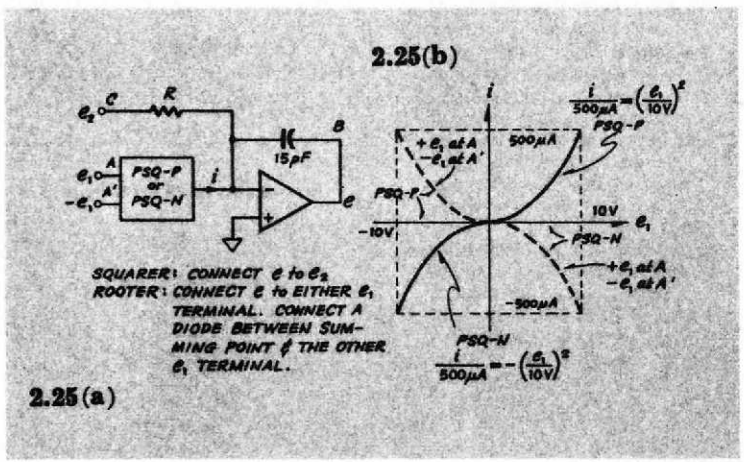
$$i = \tfrac{1}{2} \times 10^{-3}\left(\frac{e_1}{10}\right)^2 = 5 \times 10^{-6}e_1^{\,2} \qquad (2\text{-}48)$$

When used as a squarer, e is connected to e_2. The output current of this network is then transduced to a voltage (see III.30), as described by the relationship:

$$e = -iR = \frac{e_1^{\,2}}{10}\left(\frac{R}{20\ \text{k}\Omega}\right) \qquad (2\text{-}49)$$

The circuit as shown works only for positive values of e_1. If e_1 is bipolar, $-e_1$ should be connected to the other input terminal, in order to produce the desired squared output for either input polarity. (Absolute value computation is inherent in PSQ if both input polarities are supplied.) For positive *output* polarity, use PSQ-N, restricting the circuit then to *negative* input signals. II.42 shows a pair of Absolute Value circuits, either of which will convert e_1 to a single polarity, regardless of its initial intentions, and such a circuit may be used to drive either of the input terminals shown here.

*PSQ-P/N are designed to operate over a current range of 0 to 500 μA with an accuracy (@ 25°C) of: $\left|\frac{\delta i}{i_{\text{max}}}\right| < .001$ where $\delta i = i_{\text{actual}} - i_{\text{desired}}$.



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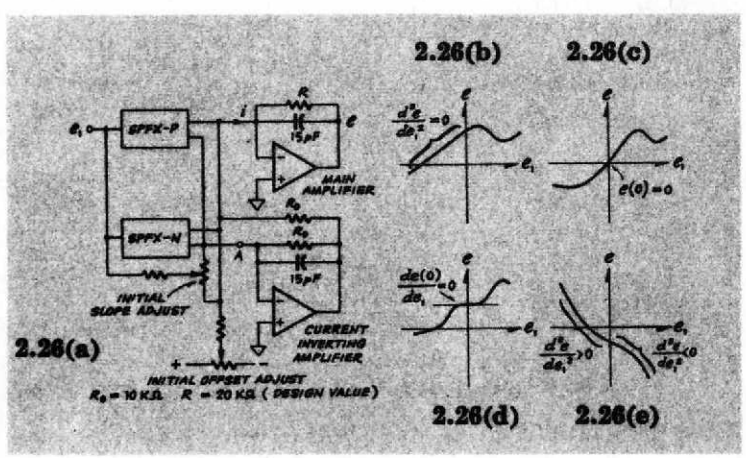
II.26 ARBITRARY FUNCTION FITTERS.

Models SPFX-P/N are ten-segment function fitters having uniformly-spaced fixed breakpoint voltages and adjustable slopes. SPFX-P has breakpoints for positive-going inputs and SPFX-N has breakpoints for negative-going inputs. Circuit (a) generates a function having inputs and adjustable slopes of either sign, and an adjustable origin. If all these degrees of freedom are not required, the circuit can be simplified; e.g., if the desired function has no slope change for one sign of input (b), one SPFX can be omitted. If the origin is at zero, (c), the initial offset adjustment is unnecessary. If the desired function has zero slope for zero input (d), the initial slope adjustment is unnecessary. Finally, if the desired function has monotonically decreasing slope (negative or zero second derivative) for a positive input and a monotonically increasing slope for a negative input (e) the inverting amplifier is unnecessary (ground point A).

The maximum slope change per straight line segment is 20 μA/volt/volt.

The amplifier output may be scaled by choosing the value of the feedback resistor R so that:

$$R\left|\frac{d^2i}{de_1^{\,2}}\right|_{\text{max}} > \left|\frac{d^2e}{de_1^{\,2}}\right|_{\text{max desired}} \qquad (2\text{-}50)$$



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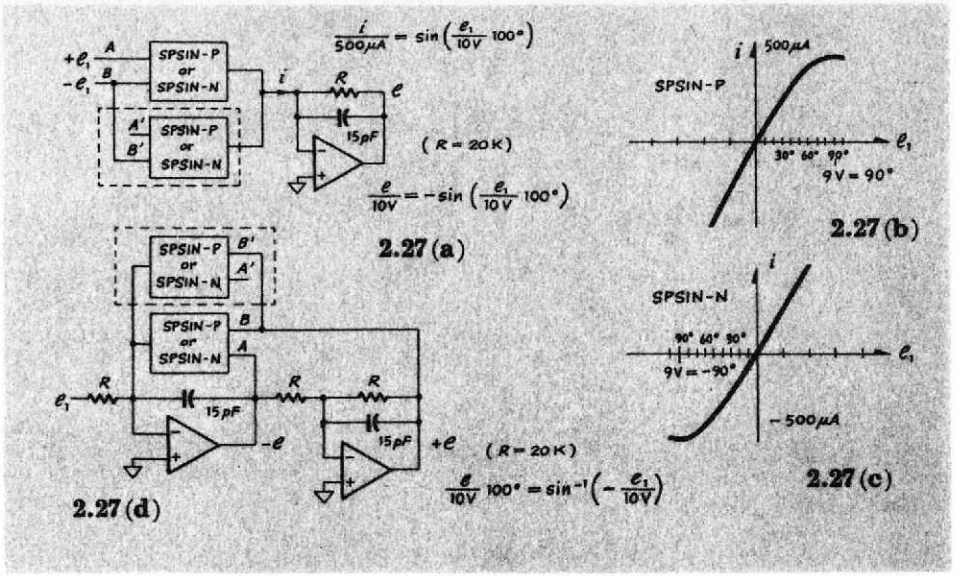
II.25

II.27 SINE-COSINE FUNCTION FITTER (SINUSOIDAL TRANSCONDUCTORS). The Philbrick SPSIN-P and SPSIN-N are diode-resistor function fitters having output currents proportional to the trigonometric sine of the input voltages.* They require two input voltages, e_1 and $-e_1$ as shown in (a). The response of the SPSIN-P is shown in (b). Since the sine is nearly the same as the angle itself for small angles, the useful range of the SPSIN-P includes small negative voltages.

SPSIN-N behaves as shown in (c).* By using a P and an N type together (additional unit inside dashed line of figure a) the sine function can be generated over a range of $-100°$ to $+100°$. Note that the polarity of the output can be changed by interchanging inputs e_1 and $-e_1$. Generation of the inverse function, arcsine, is shown in (d). In the conversion of rectangular to polar coordinate this circuit is the preferred method of generating the angular co-ordinate, for angles less than 90°. The dashed line indicates the additional unit necessary for outputs of either polarity. Both devices are scaled to 10 degrees per volt of input.

*The accuracy of both SPSIN-P and SPSIN-N (@ 25°C) is

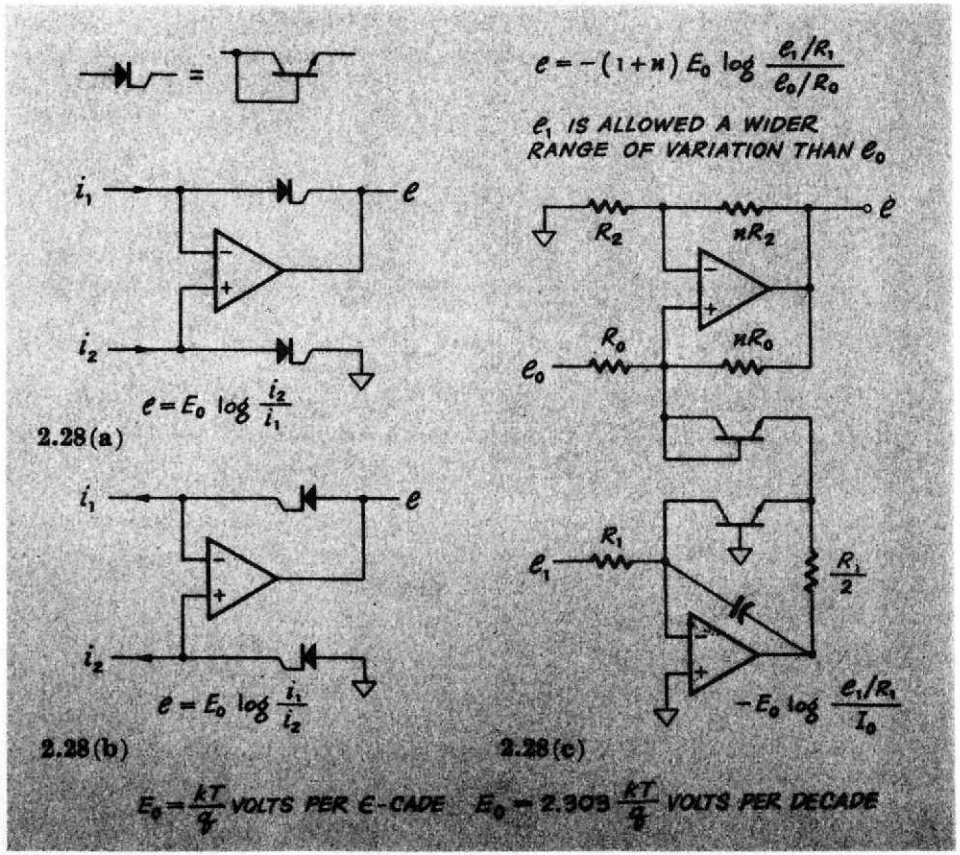
$$\left|\frac{\delta_i}{i_{max}}\right| < .001 \text{ for } -1\text{ V} \le e_i \le 10\text{ V, where } \delta_i = i_{actual} - i_{desired}$$



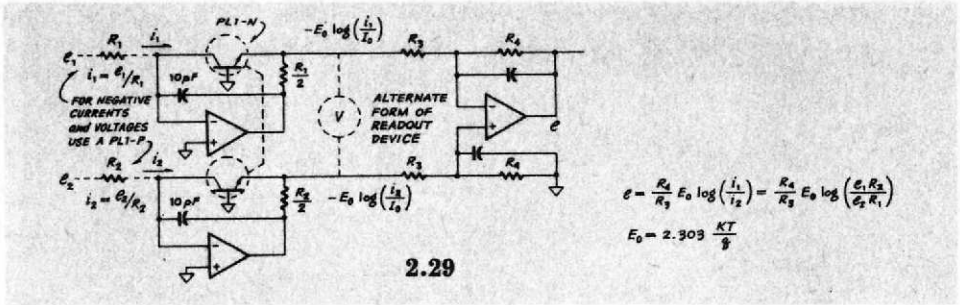
II.28 LOG OF RATIO CIRCUITS. Circuits (a) and (b) show two connections in which one may incorporate a diode-connected dual logarithmic transconductor (such as the PPL-1-N/P) and, with the aid of a differential amplifier, create an output voltage that is proportional to the logarithm of the ratio of the two input currents (note that an input voltage may not be directly converted to an input current, since the amplifier input terminals are not at ground potential). The log of *voltage* ratio will be seen later in this section. It is obvious that these circuits, although perfectly straightforward as they are drawn, have the limitation that they will operate only with unidirectional currents. It *is* possible to compute the logarithm of the ratio of input currents going in opposite directions (log of negative ratio), and it is also possible to parallel logarithmic units with those of reverse, or complementary, polarity, but please note that reversing the input polarities inverts the ratio, which is sometimes unfortunate (particularly if unsuspected).

Circuit (c) shows how to obtain the log of the ratio of two input voltages. The lower amplifier, recognizable from the discussion of II.22, computes the logarithm of the numerator (about 59 mV per decade at room temperature), and the upper amplifier functions as a current pump in the Howland Circuit (see III.6), that injects a current proportional to the denominator. The difference between the diode voltages (the log of the ratio) appears at the positive input of the Howland circuit, and is magnified by the gain ratio $(1 + n)$.

If the ratio is to a fixed quantity, one single-ended amplifier may be used with the Philbrick PPL4 P/N (or SPL4 P/N) to obtain a wideband compensated logarithm useful over 5 decades, having both slope (nominally *one volt per decade*) and reference current adjustable.



II.29 LOG OF LOW-CURRENT RATIO. This circuit is recommended for obtaining the log of the current ratio at low currents. It employs transistors in the transdiode connection, which provide at least two decades more current range than can be obtained from diode-connection of the same transistors. The subtractor that follows the two identical log-function circuits then computes the log of the ratio (the difference of the logarithms). Inputs that are current sources (such as photomultiplier tubes) tolerate larger amplifier input voltage offsets than do voltage sources. The SP2A amplifier is suitable for high-impedance (current) sources, and the SP656 for voltage sources. The output amplifier requires good common-mode rejection. Temperature variation of E_0 can be compensated by appropriate temperature coefficients for R_3.



2.29

II.29
II.22
to
II.28
II.30
to
II.33

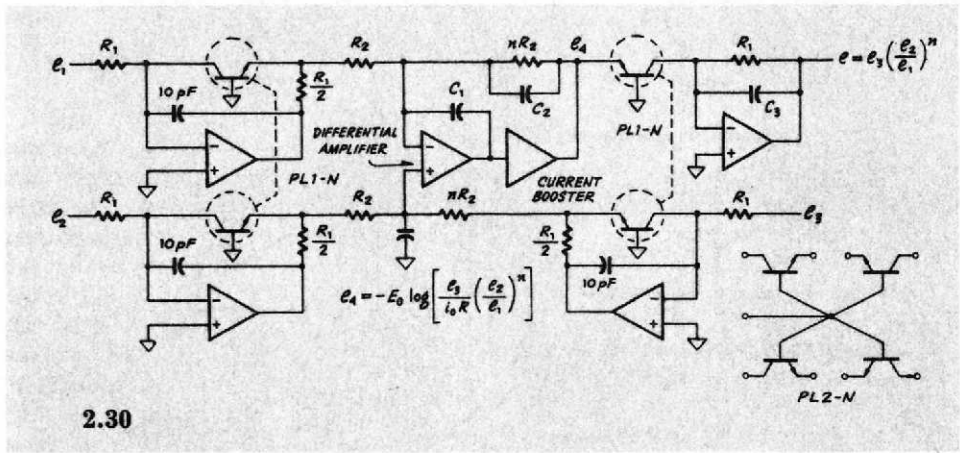
II.30 LOG MULTIPLIER CIRCUIT. This circuit produces an output of:

$$e = e_3\left(\frac{e_2}{e_1}\right)^n \tag{2-53}$$

precisely over many decades, by taking the anti-log of the signal at point e_4 which, for positive values of e_1, e_2, and e_3, is negative and of the form:

$$-E_0 \log\left[\frac{e_3/R_1}{I_0}\left(\frac{e_2}{e_1}\right)^n\right] \tag{2-54}$$

This signal is produced by feeding, to the subtractor circuit in the center of the diagram, the following inputs: (1) the log of e_1, for which it has the gain $(-n)$; (2) the log of e_2, for which it has the gain $(+n)$; (3) the log of e_3, for which it has the gain $(+1)$. Note that this is essentially a one-quadrant circuit.



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III.65
III.68

The exponent, n, is determined by the gain of the difference amplifier, which can be adjusted by changing a single resistor in a differential TEE network, (III.81) in the input circuit ($n < 1$) or feedback circuit ($n > 1$).

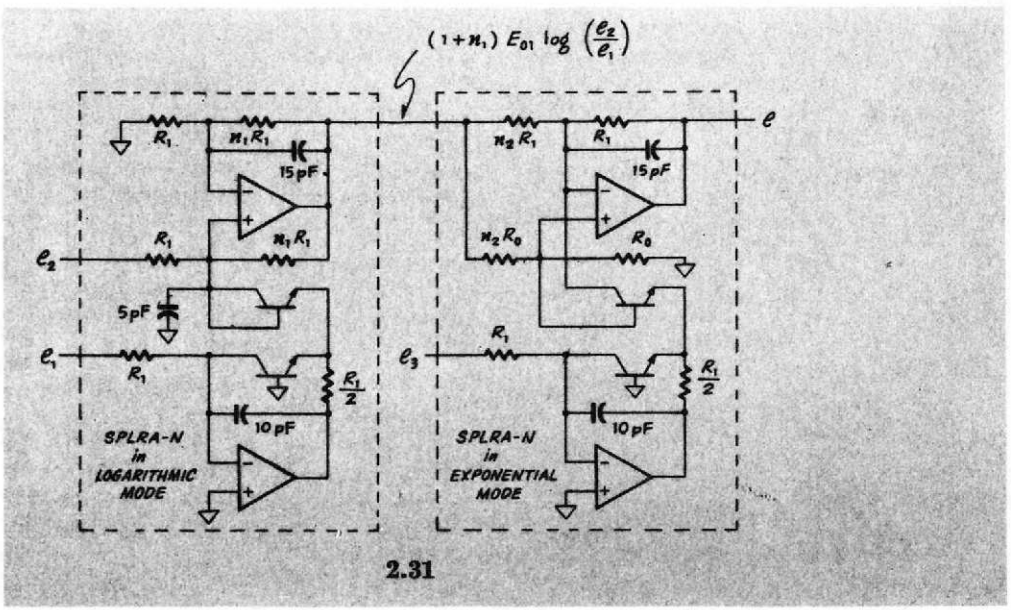
II.31 LOG MULTIPLIER (USING LOG RATIO CIRCUITS). The Philbrick Log Ratio Amplifiers (SPLRA-P or N) and Log Ratio Transconductors (SPLR-P or N) make convenient "building blocks" for a logarithmic multiplier. The circuit shows two SPLRA-N Log Ratio amplifiers connected to give an output

$$e = e_3\left(\frac{e_2}{e_1}\right)^n \quad \text{where} \quad n = \frac{(1+n_1)E_{01}}{(1+n_2)E_{02}} = \frac{(1+n_1)T_2}{(1+n_2)T_1} \tag{2-55}$$

The transconductor version is the same, except that the lower amplifier in each unit must be provided separately. The gains of the two units, $(1+n_1)$ and $(1+n_2)$ are used to compensate for any slight differences in the junction temperatures (T_1, T_2) of the two units, or alternately can be adjusted to give n any value between approximately 1/5 and 5. Transistor mismatch error appears as a constant scaling error in one or more of the inputs and can be removed by changing the gain of the affected inputs (small adjustable resistors in series with each input is the simplest method). When these adjustments are made accuracies of the order of

$$\left|\frac{\delta e}{e_{\text{desired}}}\right| \ll .001 \qquad \delta e = e_{\text{actual}} - e_{\text{desired}} \tag{2.56}$$

can be obtained over three decades of input voltages. The circuit shown works for positive input voltages. Use SPLRA-P for negative inputs.



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II.32 QUARTER-SQUARE MULTIPLIER. All of the circuitry to the left of the dashed line is devoted to adding, subtracting, and weighting e_1 and e_2 (by what should be, at this point, thoroughly familiar techniques) to produce the four signals that are fed into the PSQ-N and PSQ-P squaring circuits, the outputs of which are fed to the inverting adder that completes the circuit. The few lines of algebra that follow prove that the output will, indeed, be proportional to the product of e_1 and e_2.

$$i_a = -\,(.5\text{ mA})\left(\frac{e_1 + e_2}{20\text{ V}}\right)^2$$

$$i_b = (.5\text{ mA})\left(\frac{e_1 - e_2}{20\text{ V}}\right)^2 \qquad (2\text{-}57)$$

$$-e = (20\text{ k}\Omega)(i_a + i_b)$$

$$e = (10\text{ V})\left[\left(\frac{e_1 - e_2}{20\text{ V}}\right)^2 - \left(\frac{e_1 + e_2}{20\text{ V}}\right)^2\right] = \frac{e_1 e_2}{10\text{ V}}$$

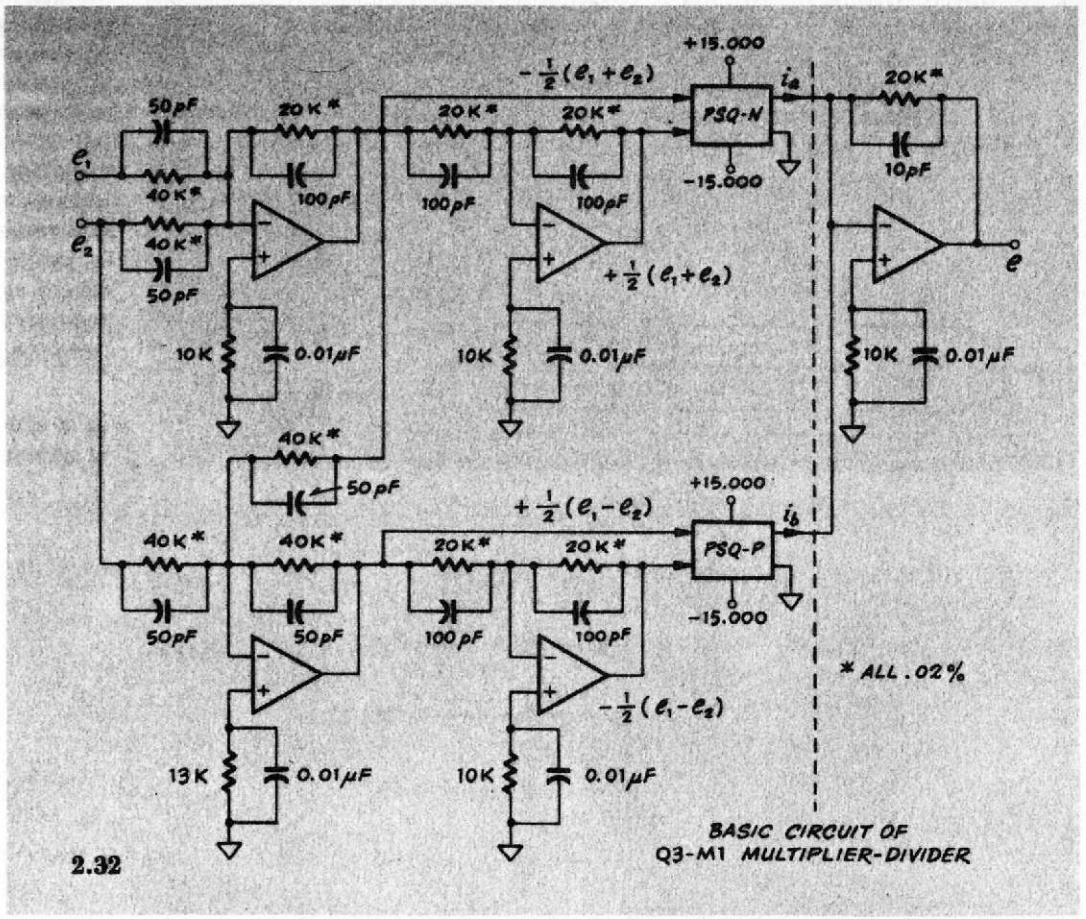
Note that this circuit is a true *four-quadrant* multiplier, capable of producing an output of either polarity, as demanded by any arbitrary combination of the polarities of e_1 and e_2.

When high-speed amplifiers are used (such as the P65AH) the frequency response of the multiplier is limited by the squaring circuits, the time constant of which is approximately 0.3 μsec.

By interchanging the PSQ-P and PSQ-N the output polarity is changed, giving

$$e = -\frac{e_1 e_2}{10\text{ V}} \qquad (2\text{-}58)$$

This circuit may also be used to accomplish division, and the next Section is devoted to that subject.



II.32
II.22 to II.31
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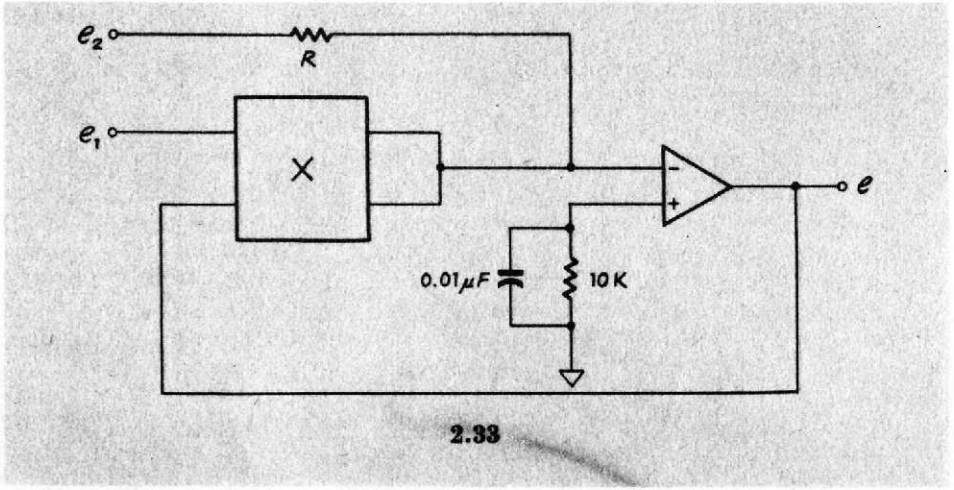
III.63
III.64
III.65
III.68

II.33 QUARTER-SQUARE DIVIDER. If we represent all of the circuitry to the left of the dashed line in figure 2.32 by a rectangle marked "×," then the circuit shown here is an effective divider; that is:

$$e = \left(\frac{20\text{ k}\Omega}{R}\right)\left(10\text{ V}\,\frac{e_2}{e_1}\right) \qquad (2\text{-}59)$$

There is very little difference between this circuit and that of the multiplier of II.32, except that the output of the final summing amplifier is connected back to one of the old multiplier inputs, and the other input (e_2) is fed directly into the summing point through a resistor of appropriate value for correct weighting. One degree of freedom has been lost, however: the polarity of e_1 must now be negative. (If the output polarity has been changed by interchanging the PSQ-P and PSQ-N then e_1 must be positive.) In all other respects, the accuracy and range of the multiplier circuit of II.32 are preserved. Output errors increase in inverse proportion to e_1.



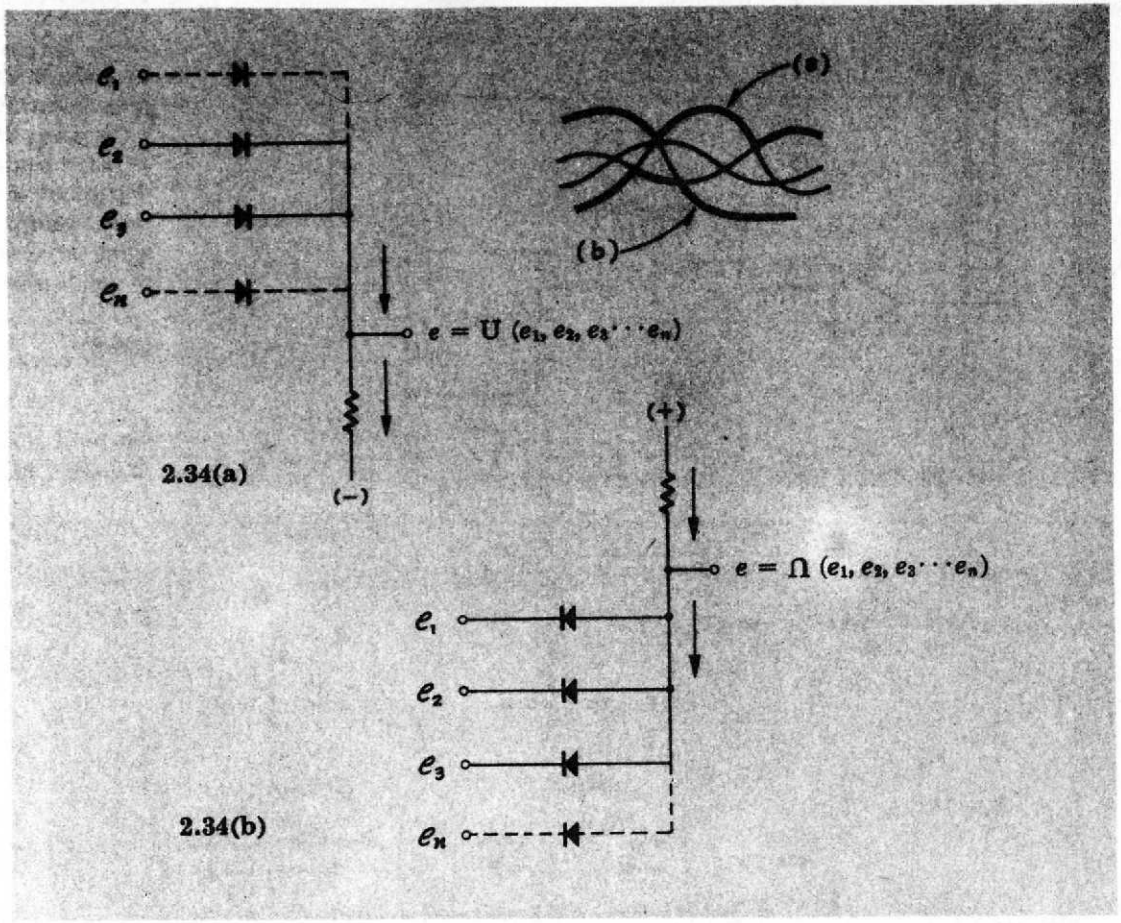
II.33
II.22 to II.32

II.34 ELEMENTARY SELECTOR CIRCUITS. In circuit (a), the output voltage will always be at a potential equal to the highest of the input voltages, minus the diode drop. Thus, (except at near equality) only one diode can conduct at any instant, and at least one *must* conduct, assuming that the negative supply is lower in potential than any of the inputs may ever be. The resistor is proportioned to provide sufficient current to maintain adequate speed at the lowest voltage, yet limit the diode current to a specified maximum value for the *highest* voltage anticipated. For fast switching circuits, it is best to design for as much diode current as can comfortably be allotted to the Selector Circuit, so that stray capacitance effects are minimized.

The output of circuit (b) is always equal to the lowest input voltage, *plus* the diode drop. Once again, we assume that no input voltage can be higher than the positive supply, and we advocate designing for the highest comfortable diode current.

To achieve compensation that is independent of signal amplitude, even when the largest signal is very close to the return supply in magnitude, we recommend constant-current sources instead of resistors—see III.9.

The Upper Selector can be thought of as presenting at its output the most positive (or least negative) of its input voltages. As shown in 2.34(b) it presents to its output the "upper envelope" of all the input signals. Similarly, the lower selector presents to its output the most negative (or least positive) of its inputs, i.e., the "lower envelope" of all the input signals.



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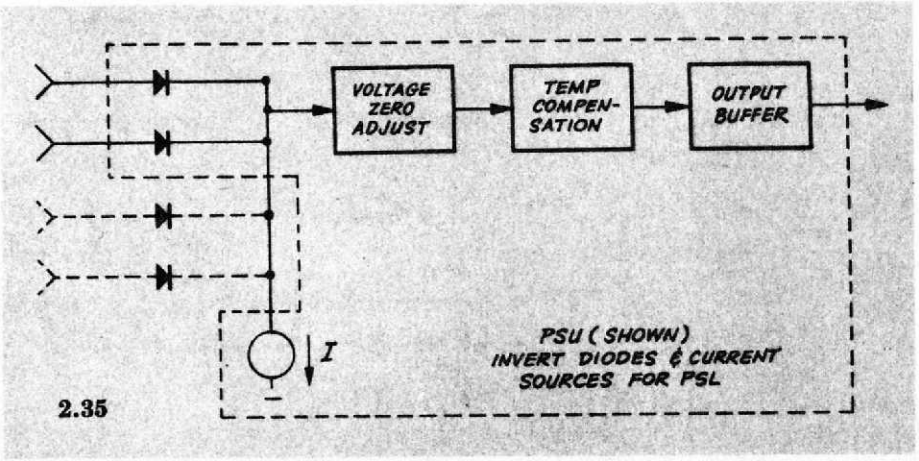
III.74
III.79
III.81

II.35 COMPENSATED SELECTOR. Although Selection is simple enough in concept, Selector circuits require certain refinements if their performance is to approach the ideal described in II.34.

These features are incorporated in Philbrick standard Upper and Lower Selectors, designated the PSU and PSL respectively. As shown here, a constant-current source (I) draws current from one or the other of a pair of diodes. The diodes are carefully matched at the current level established by the source. (If Selection among more than two voltage variables is required, the user may connect additional diodes of a recommended type to the selection node.) A voltage adjustment is included in the PSU/PSL design, enabling the user to establish zero output for zero input. This is done by grounding one input, leaving the other(s) open, and adjusting for zero output. The temperature compensation provided in the PSU/PSL design achieves thermometric insensitivity comparable to that of wirewound resistors. Finally, an output buffer amplifier aids error-free cascading of Selectors and provides adequate output-current capability for driving computor amplifier inputs.



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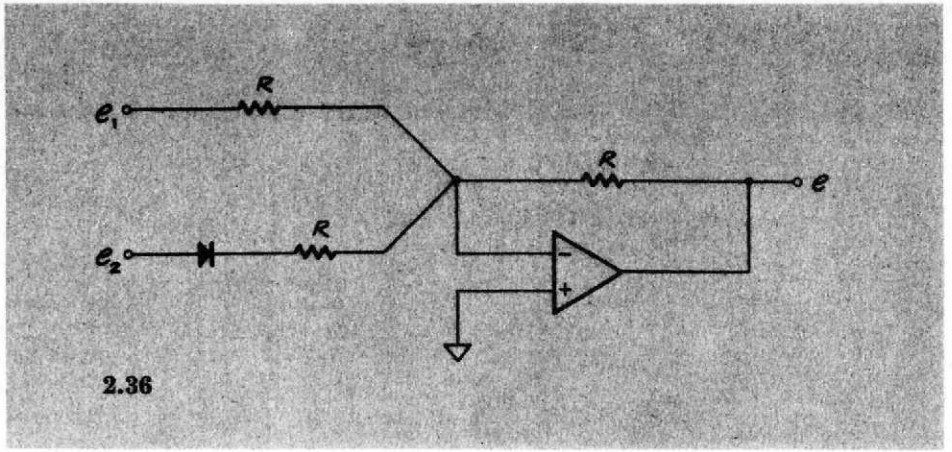
II.36 SIMPLE DUAL-MODE CIRCUIT. The only difference between this circuit and the inverting adder of II.3 is the diode in series with e_2. The basic rules must still be followed, of course, so that the sum of the input currents must equal the feedback current, and the summing point must be very close to ground—removed only by the residual null voltage. If both inputs are positive, the output is simply the negative of the sum of the two (ignoring the diode drop). On the other hand, if e_2 is negative, or if both are negative, the output is simply equal to the negative of e_1. This circuit, therefore, has two modes of operation, the choice of which depends upon the polarity of e_2 with respect to ground—with $e_2 > 0$, the circuit is an inverting adder; and, with $e_2 < 0$, it is merely a unity-gain inverter with respect to e_1 only.

In particular, if e_2 and e_1 are identical, the gain will be different for positive or negative input. Accuracy can be improved through use of a Selector circuit (see II.34, II.35), to reduce or eliminate the effect of diode drop.



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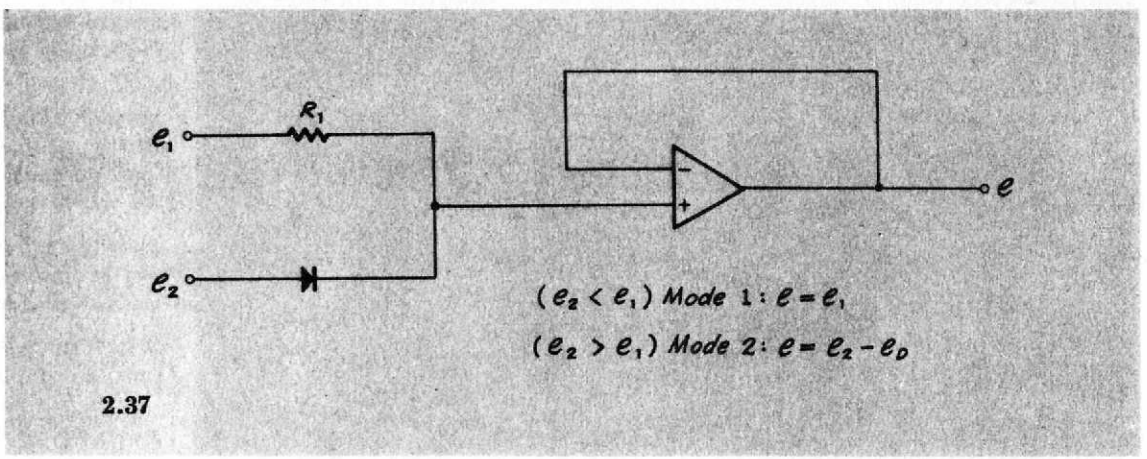
III.50
III.63
III.74
III.75
III.81

II.37 SIMPLE DUAL MODE CIRCUIT (Non-Inverting). This circuit will be recognized as a simple follower having two inputs. If e_2 is more positive than e_1, the output is equal to e_2, ignoring the diode voltage drop.

When e_2 is negative with respect to e_1, the output is equal to e_1, and the specific value of e_2 has no effect on the output, provided that it is sufficiently negative to render the diode leakage current negligible. (The path for this leakage current, by the way is mostly through R_1.) The accuracy and speed can both be improved by use of a Selector circuit.



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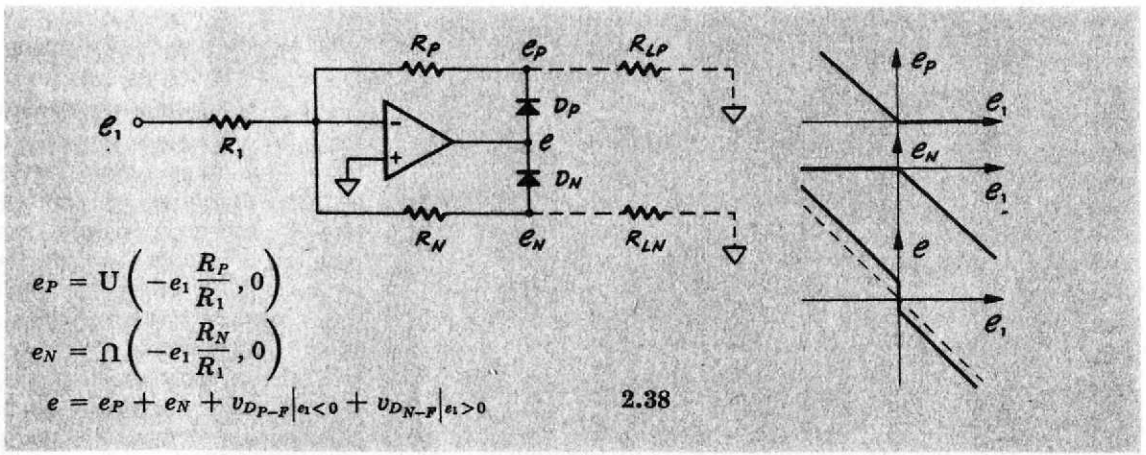
III.74
III.75
III.81

II.38 SIGNAL POLARITY SEPARATOR. This circuit is important for low voltage applications because it provides precisely-scaled selection of the input, e_1, with respect to ground potential, at the outputs e_P and e_N.

When D_P is not conducting, e_P is nearly zero, assuming resistive loads returned to ground (or to the virtual ground of a single-ended amplifier). The departure of e_P from zero will depend upon the reverse current of diode D_P through R_P in parallel with R_{LP}. This error can be made small and virtually constant by making R_N zero.

When D_P is conducting, the error at e_P is the forward voltage across D_P *divided by the amplifier gain*. Hence, precise selection may be accomplished, even when e_1 is in the millivolt range.

As an added feature at the selection point ($e_1 = 0$) the output e undergoes a sharp transition which may be differentiated and used as a logic signal for commanding gates or relays.



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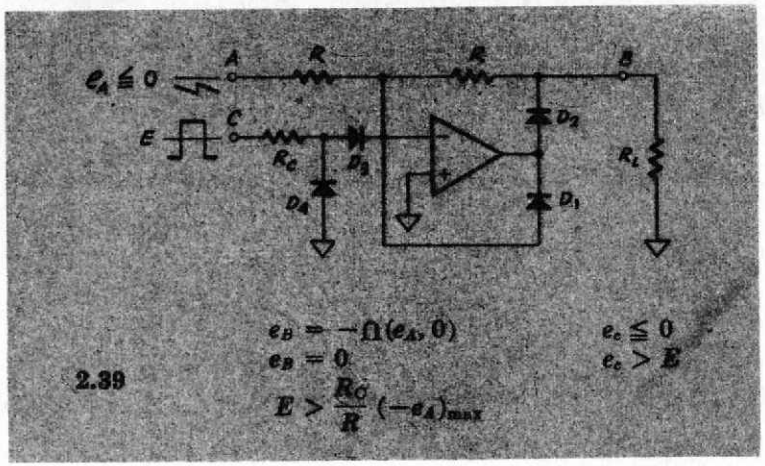
to
II.37
II.39
to
II.44

II.39 PRECISION GATE. When this gate is "closed" it functions as a normal unity-gain inverter between terminals A & B, for *negative* input signals. Positive input signals result in no output, because they would tend to swing the amplifier output terminal negative, which is prevented by the cooperative bounding action of D_1 and D_2. When the gate is "open," terminal A is isolated from terminal B.

The gate is swung open and shut by application of a signal to terminal C. Assuming that the resistor (R_C) in series with terminal C is small compared to R, a positive signal of any appreciable magnitude applied to C will cause the circuit to clamp in the condition in which D_1 bounds it, and D_2 disconnects the amplifier from terminal B. If terminal C is open-circuited, or returned to ground, or if a negative signal is applied to terminal C, the gate is closed, and the A-to-B circuit acts like a normal unity gain inverter . . . but as mentioned above, only for negative input signals applied to A. Positive input signals applied to A will open the gate, just as if they had been applied to terminal C. Note that the "closed resistance" of this switch approaches zero, to the extent that the inverter performance approaches the ideal. When the switch is open, the isolation is nearly as perfect, being somewhat dependent upon the leakage in D_2.

As in II.38, loads must be resistive and grounded.



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III.74
III.75
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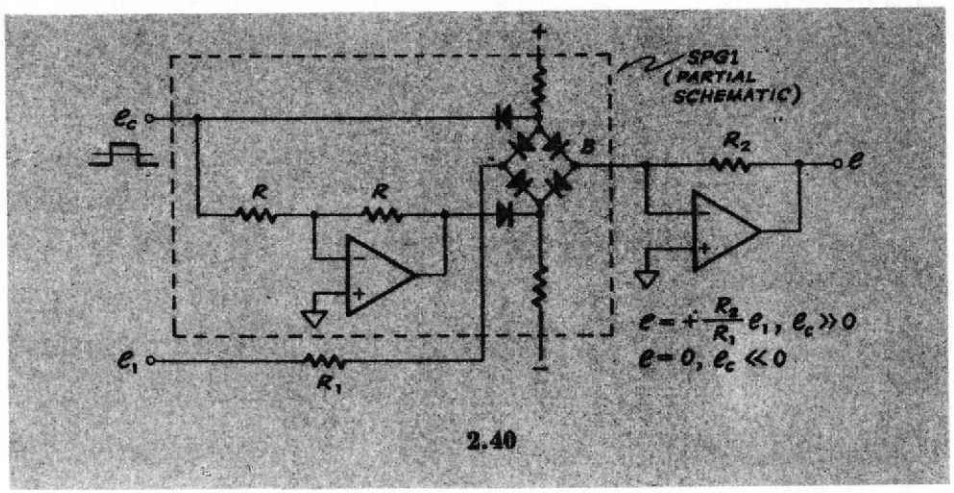
III.81

II.40 ELECTRONIC SWITCH. In this circuit, e_1 is gated to point B when, and only when $e_c \geqq 1$ volt. The unity-gain inverter produces $-e_c$ at the lower end of the diode bridge when $+e_c$ is applied as shown; and, provided the magnitude of e_c is of the order of 2 volts or more, the bridge becomes conducting from e_1 to B. Negative values of e_c ($e_c \leqq -1$ V) render the bridge non-conducting.

An application to which this circuit is ideally suited, and often applied, is the resetting or clamping of integrators. In such applications the corner of the bridge nearest "e_1" is connected to the output of the integrator, and the opposite corner is connected (as shown in our diagram) to the summing point.

The reader who prides himself on commercial awareness will not be at all surprised to learn that Philbrick makes available a module, called the SPG1, in which not one, but *two* of these splendid circuits, are economically presented, in a neat and painless package.*

*The SPG1 contains two complete diode bridges, and a driver stage; a single logic signal "inhibits" one bridge, "enables" the other, or vice versa, according to the signal polarity. The two bridges may be used, for example, instead of the relay circuit of II.50, for setting arbitrary initial conditions.



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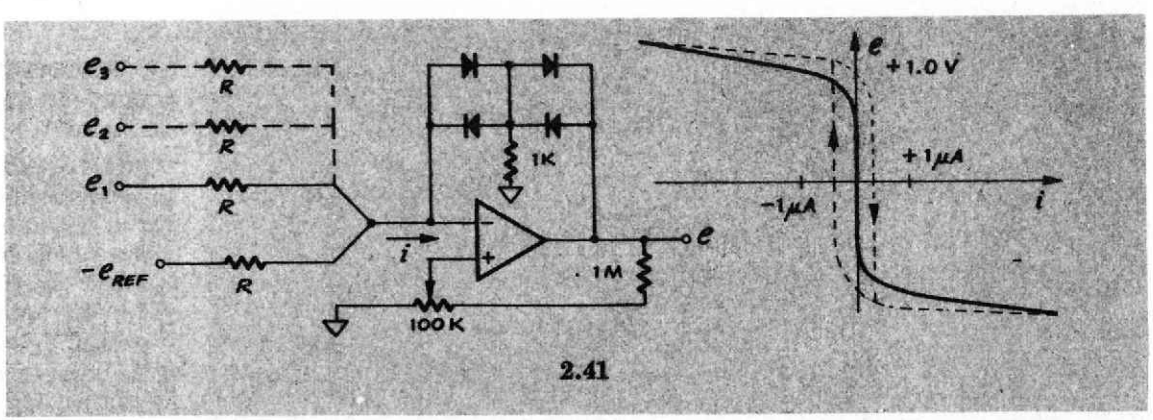
III.81

II.41 PRECISION COMPARATOR. This circuit indicates whether a voltage is greater than or less than a desired reference voltage. It does so by sensing the direction of the current, i, flowing between the input network and the amplifier summing point, and bounding the output accordingly. Since the circuit is current-sensitive, it can just as easily compare the sum of several voltages against a reference, or for that matter, against the sum of several references. Note that the reference voltage, although it need not be constant, does need to be inverted before being presented to the comparator. The output is approximately logarithmic, providing a graded null.

For very *slowly* changing voltages, "snap action" can be added by means of positive feedback, at the small price of introducing a finite amount of hysteresis. The amount of hysteresis is controlled by the potentiometer connected to the positive input (which should be grounded if snap action is not required).



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to
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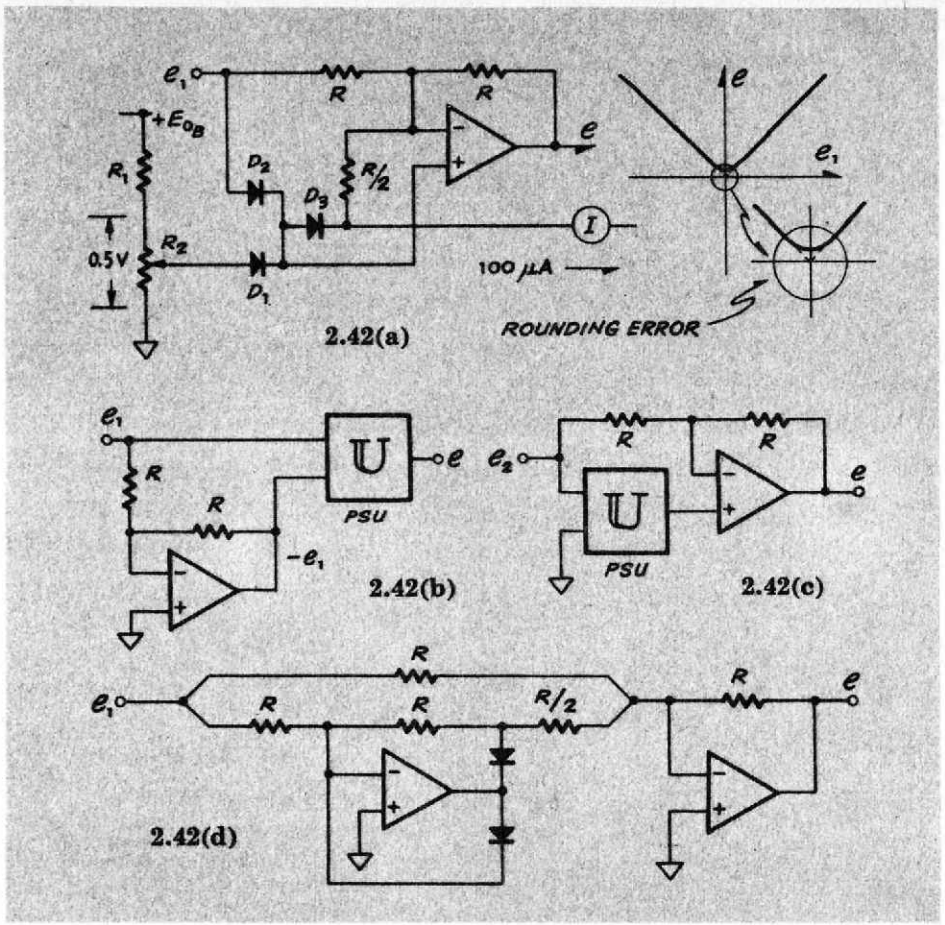
III.43
III.44
III.45
III.58

II.42 SIMPLE ABSOLUTE-VALUE, PRECISION ABSOLUTE-VALUE CIRCUIT. With negative input, the positive terminal of the amplifier in (a) is as close to ground potential as one can adjust the low-resistance potentiometer. Hence, negative-polarity signals find their way from e_1 to e through a unity-gain inverter. Positive-going signals have three paths. One is via the unity-gain inverter. Another is via the drop of D_2 to the positive input, whence a gain of $(+4)$ is realized for $(e_1 - V_{D2})$. The third is via D_2 and D_3 in series with $R/2$, whence a gain of (-2) is obtained for $(e_1 - V_{D2} - V_{D3})$. The sum of these terms is simply e_1, if $V_{D2} = V_{D3}$ at the suggested current. The output is, thus, a positive-going signal, equal in magnitude to the input, but of positive polarity, *regardless* of the input polarity. (If, for example, e_1 were to be a sine wave, e would be the positive full-wave-rectified version of it.) If all diode and supply polarities were reversed, one would obtain the *negative* absolute value. The Philbrick PSU Upper Selector is used to obtain the absolute value in 2.42(b) and 2.42(c). In the PSU, a zero adjustment, for diode-difference compensation, is incorporated within the unit. In (b), the Selector is presented with the input voltage and its negative, and presents the greater of them at the output. A (single-ended) amplifier is required to invert the input, if its negative is not already available in the system. In (c), the PSU selects accurately between the input and ground, presenting the greater of them to the positive input. When the input is negative, inverter action takes place, because the positive input is at ground potential; when the input is positive, follower action occurs. A good differential amplifier is needed in (c), but all the advantages of a feedback amplifier are gained, including the possibility of inserting a booster in the loop for high current capability.

By placing the diodes within the feedback loop, the circuit of 2.42(d) renders them effectively "ideal." When e_1 goes negative, the output of the first amplifier jumps positive by one diode drop, shutting off the upper diode and bounding the amplifier through the (conducting) lower diode. The second amplifier simply inverts the (negative) e_1. When e_1 is positive, both amplifiers invert and the output is: $e = 2e_1 - e_1 = +e_1$, by virtue of the gain of 2 in the lower branch.



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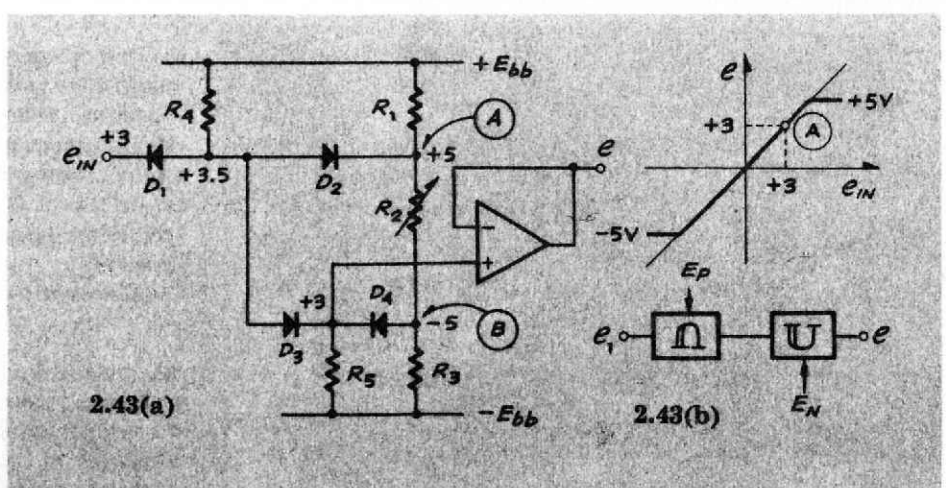
III.63
III.64
III.65
III.81

II.43 CLIPPER. This circuit has, in the Ideal Case, linear and unity-gain response between two sharply-defined limits, above and below which its output is constant at the limit value; thus it behaves as a "clipper," without saturation of the amplifier or other undesirable side effects. The curve illustrates its Ideal behavior for symmetrical limits of ± 5 V. R_2 adjusts both limits simultaneously.

For convenience in analyzing circuit performance, we have annotated the schematic with typical voltage values, representing the prevailing conditions for a +3 V input (point A on the curve). Under these conditions, D_1 and D_3 are conducting, and D_2 and D_4 are not. Above $e_{in} = 5$ V, D_2 conducts, clamping the output at +5 V. Below $e_{in} = -5$ V, D_4 conducts, clamping the output at -5 V. For good accuracy, the forward drop of D_1 should match that of D_3 . . . a condition that could be encouraged by replacing R_4 and R_5 by constant-current sources (cf: II.35 and III.8), particularly if the signal excursion approaches E_{bb} in magnitude. When in lower bounds, diode drop in D_4 is not compensated. N.B. Selector units PSL & PSU will provide bounds having accuracy, temperature and diode-difference compensation, and low output impedance—*sans* amplifier!



II.43
I.25
I.32
II.34
to
II.42
II.44
III.8
III.15
III.58
III.66
III.67

II.44 DEAD ZONE. This circuit establishes a region of almost complete insensitivity to small values of input.

$$-E\frac{R_2}{R_1} < e < E\frac{R_4}{R_3} \qquad (2\text{-}59)$$

In that region, both D_1 and D_2 are reverse-biased. D_3 and D_4 limit the reverse bias, and hence block both the leakage current and any stray capacitive coupling from the input terminal to the amplifier.

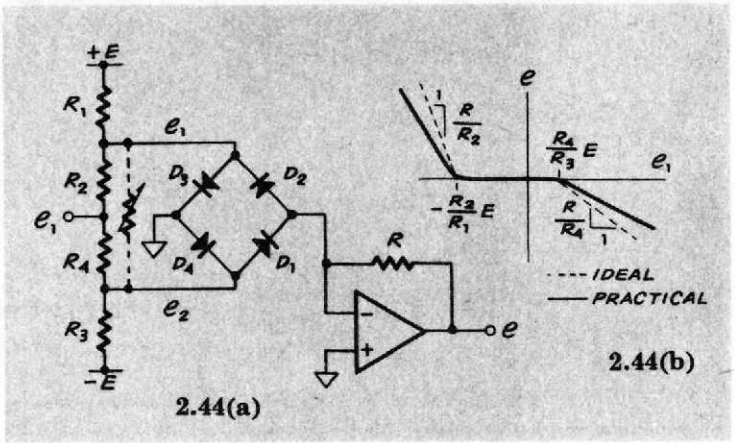
When e_1 becomes sufficiently large, D_1 or D_2 conducts. The output voltage is approximately:

$$e = -\frac{R}{R_2}\left(e_1 + \frac{R_2}{R_1}E\right), e_1 \text{ neg.} \qquad (2\text{-}60)$$

$$e = -\frac{R}{R_4}\left(e_1 - \frac{R_4}{R_3}E\right), e_1 \text{ pos.} \qquad (2\text{-}61)$$

In both expressions, diode offset has been neglected. Its principal effect is to cause significant rounding at the corners of the response characteristic, as shown. Practical values for R_3 and R_1 may be larger than the equations would indicate.

Further, these offsets are temperature-dependent (2–3 mV/°C referred to input), a source of uncertainty in the intercepts of the characteristic. D_1 and D_2 may each be replaced by an "ideal diode" (or polarity separator) circuit like that of II.38, virtually eliminating the effect of diode offsets. The dashed resistor—when used—permits symmetrical adjustment of the thresholds by means of a single adjustable element.

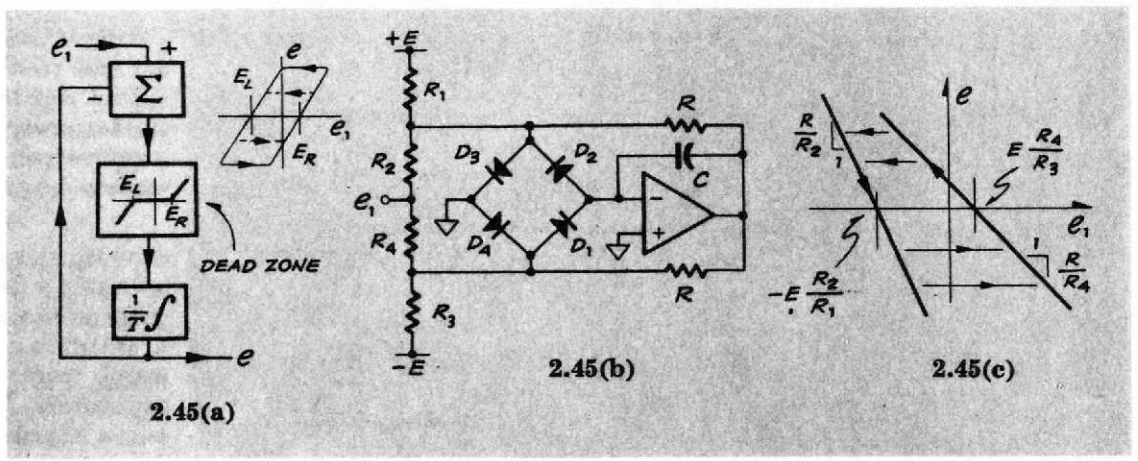


2.44(a) 2.44(b)

II.44
I.32
II.34
to
II.43
III.58
III.77
III.79

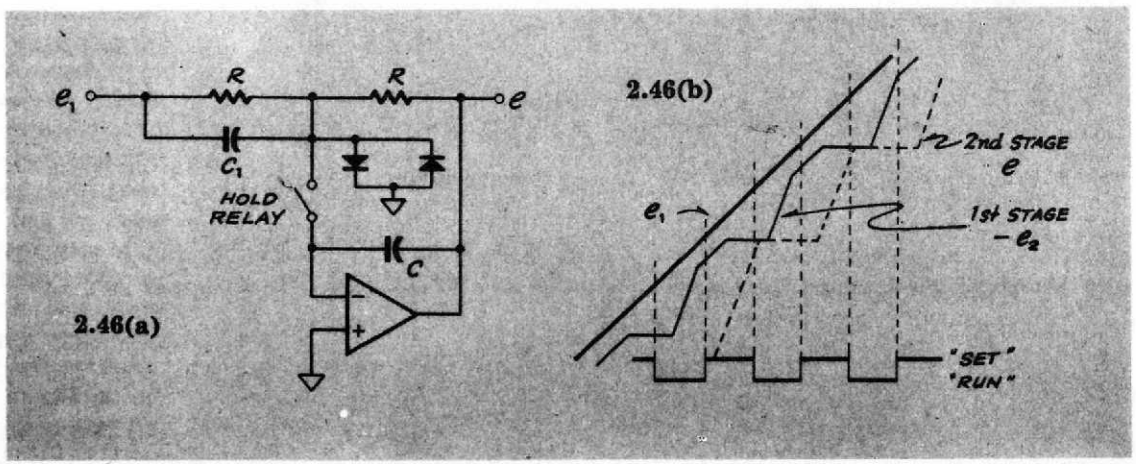
II.45 BACKLASH SIMULATION. Backlash (often called hysteresis) may be simulated by applying a circuit having the dead-zone characteristic described in II.44 to a feedback loop like the one shown in (a). Circuit (b) is a practical realization of 2.44(a), providing the required summing and integrating capabilities.

When the input is changing, and the output is beyond the transition region the output lags the input in a manner determined by the time constant RC. (To minimize this lag, minimize RC.) When the output is in the transition region (diodes D_1 and D_2 both reverse-biased) the output drifts at a rate equal to the net leakage current into the summing point divided by C. Hence, the diodes, the amplifier, and the capacitor should be chosen for minimum leakage. The choice of C must therefore reflect a compromise between tracking speed and holding accuracy.



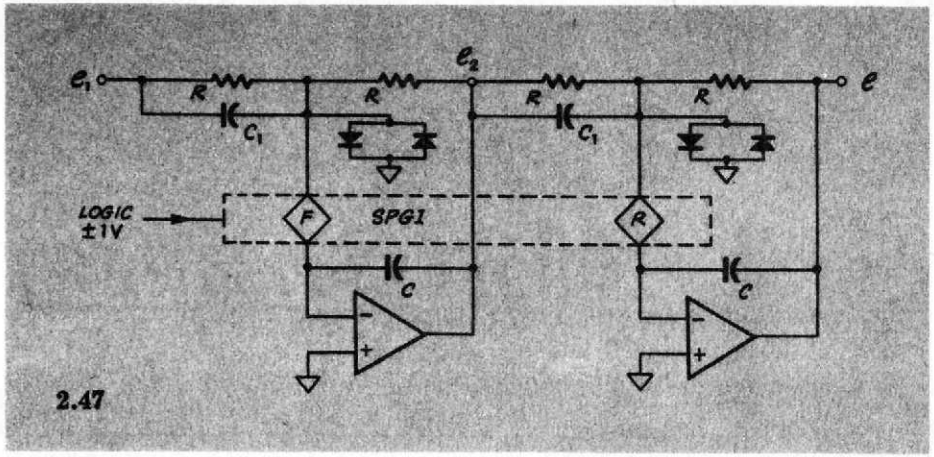
II.45
III.77

II.46 TRACK AND HOLD MEMORY (Relay Switching). The Philbrick SPREL set-hold relay pair is an excellent way of equipping an integrator with Track-and-Hold capability, using circuit (a). Choose C to achieve the hold accuracy required (see II.10 and II.11). R must be low enough in resistance so that RC is a small enough time constant to permit accurate tracking of the fastest-changing signal expected. The capacitor C_1 can be chosen so that the ratio of the feedback time constant to the input time constant is the same as the ratio of the closed-to-open switching times of the relay. The second relay in the SPREL operates in a complementary manner to the first and can be used in a second-stage track-hold circuit, by driving the logic input appropriately. (Two stages of Track-Hold are often required so that the second can hold the previous result while the first is taking a new sample.) The ramp response typical of a two-stage circuit, is shown in (b).



II.46
I.33
I.34
I.36
II.47
III.53
III.56
III.57
III.74
III.75
III.76

II.47 TRACK-HOLD MEMORY (Electronic Switching). The Philbrick SPG1 (see II.40) can be used to replace the SPREL circuit of II.46. In the circuit shown here, which embodies two stages, as suggested in II.46 C_1 must equal C, since the diode switch operates virtually instantaneously . . . at least in comparison with the RC time constants. The major disadvantage of this circuit is the required long recovery (sampling) time, while the output relaxes exponentially (following the RC feedback time constant) from the value it had in the previous Hold state to the value it must have in the Track state. This problem can be largely eliminated by using the circuit of II.48. Leakage in the Hold mode may be a problem, particularly at high temperatures. The Waveforms that would describe the behavior of 2.47 are similar to those in Figure 2.46(b), except that there is no relay-operating-time delay.

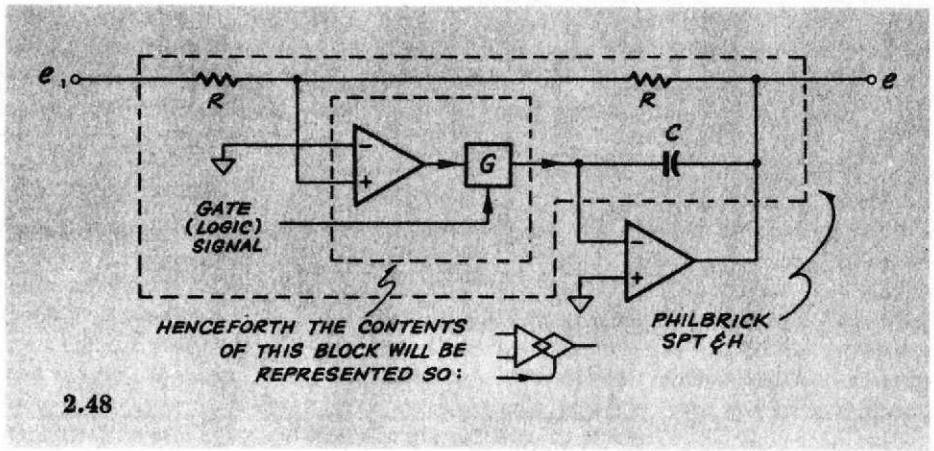


2.47

II.47
I.33
I.34
II.40
II.46
II.48
III.49
III.50
to
III.53
III.74
to
III.76

II.48 TRACK-HOLD MEMORY (Gated Amplifier). Here a gated amplifier replaces the electronic switch used in II.47, and the relay used in II.46, as the device that shifts the circuit from the Track mode to the Hold mode. Used as a current amplifier, to increase the speed of tracking by providing more charging current, it need not have voltage gain. It must be non-inverting, and, when gated off, must exhibit as little leakage as possible to the amplifier input. For stability, it must have little phase shift up to the maximum frequency for which the loop gain of the amplifier-*cum*-integrator is greater than unity, and must have at least as small input uncertainty as the computing amplifier, though its input leakage current is less important.

Anticipating your desire for a convenient and economical "black box" we have invented the Philbrick SPT&H, which will also perform peak—and valley—following operations, at the flick of a switch. (See III.53.)

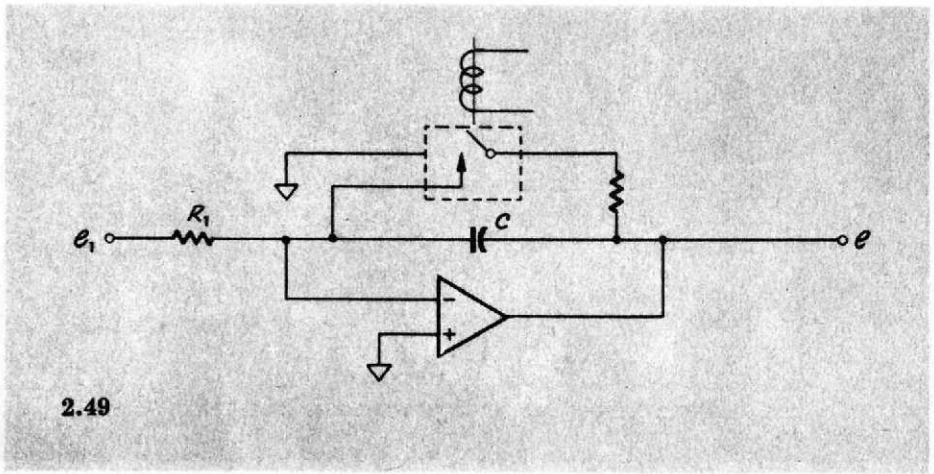


2.48

II.48
I.33
I.34
II.39
II.46
II.47
II.51
III.49
to
III.53
III.74
III.75
III.76

II.49 ZERO-VOLT RESET. Integrators must be reset to appropriate initial conditions, before each new computing cycle begins. Here we show a relay discharging the feedback capacitor to zero, thus resetting the output to zero. A small series resistor limits the capacitor discharge current to protect the relay contact and the capacitor. This resistor should be no larger than necessary, since it can allow the circuit to reach an equilibrium significantly different from zero, if its resistance is significant with respect to R_1.

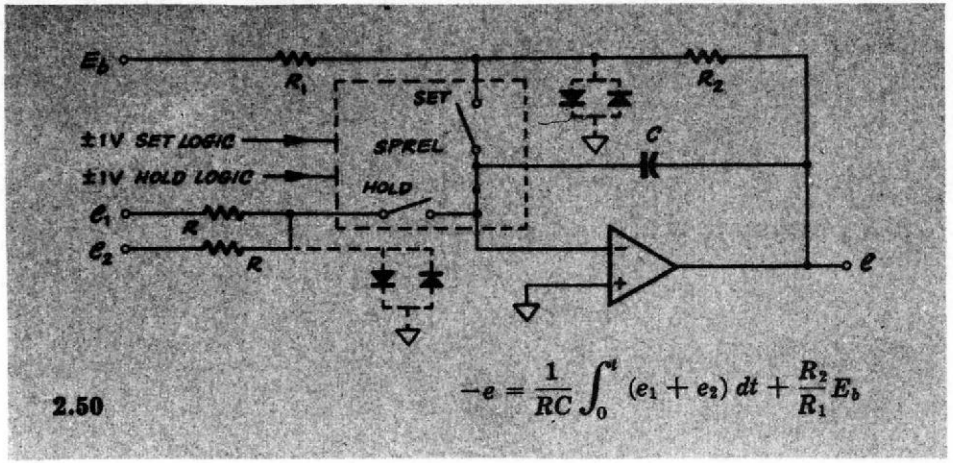
Three *caveats:* (1) Minimize leakage across the relay contacts, or the circuit will approach the function of a high-gain unit-lag, rather than a true integrator; (2) Poorly-chosen relay coils may induce an "inductive kick" into surrounding circuitry, unless damped. This occurs when the relay is deenergized (the worst possible time—just as integrating begins again); (3) Leakage and stray capacitance from the relay drive potential to the summing point can be far more serious than leakage across the contacts, because that voltage can be as high as the power supply. Hence, this switch should be appropriately shielded and grounded.



2.49

II.49
I.34
I.36
II.10
II.12
III.46
III.75
III.76

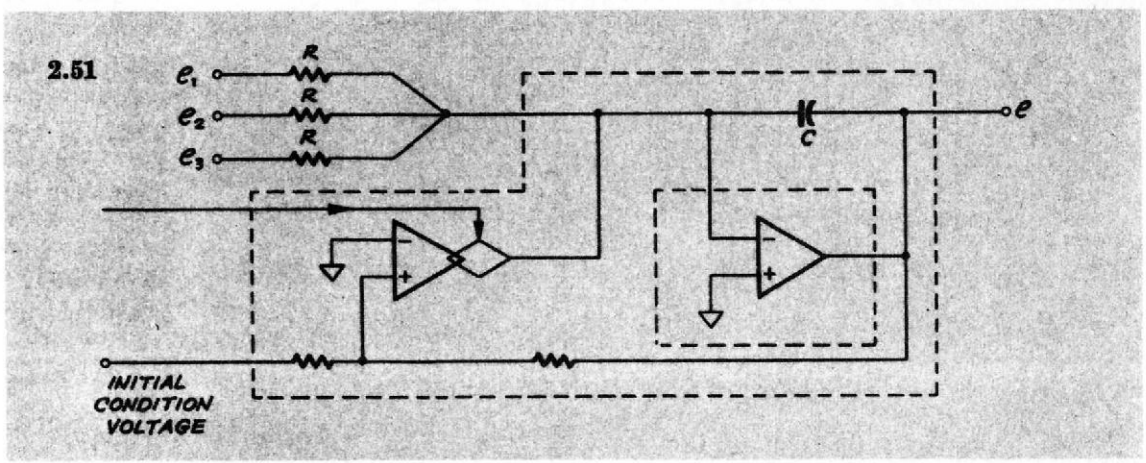
II.50 INITIAL CONDITIONS RESET. The Philbrick SPREL set-run reed relay pair is designed for this application. Resetting will be accomplished with the time constant R_2C; hence, R_2 must be low for fast reset. However, the R_1, R_2 network must not be so low in resistance as to overload either the amplifier or the initial-condition source, E_b. Independent logic input signals may be fed to the SPREL to control the Set and Hold modes. The diode clamps shown in dashed lines will help to reduce both AC and DC leakage currents across the relay.



II.50
I.33
I.34
I.36
II.10
II.49
II.51

II.51 INITIAL-CONDITIONS RESET (Gated Amplifier). Here we show a gated amplifier (non-inverting), used as a means of very quickly resetting a summing integrator to an initial condition. The circuit is identical in function to that of II.50, except that the gated amplifier is inherently faster than the relay, and the integrating network is not disconnected, because the gated amplifier has established a new summing-point for the Reset condition. See II.39.

The Philbrick SPT&H may serve in this capacity as well, provided that its built-in 0.01 μF integrating capacitor is suitable. Larger capacitors may of course be connected externally and will then be in parallel with the 0.01 μF already inside the SPT&H.



II.51
I.33
I.34
II.10
II.12
II.49
II.50