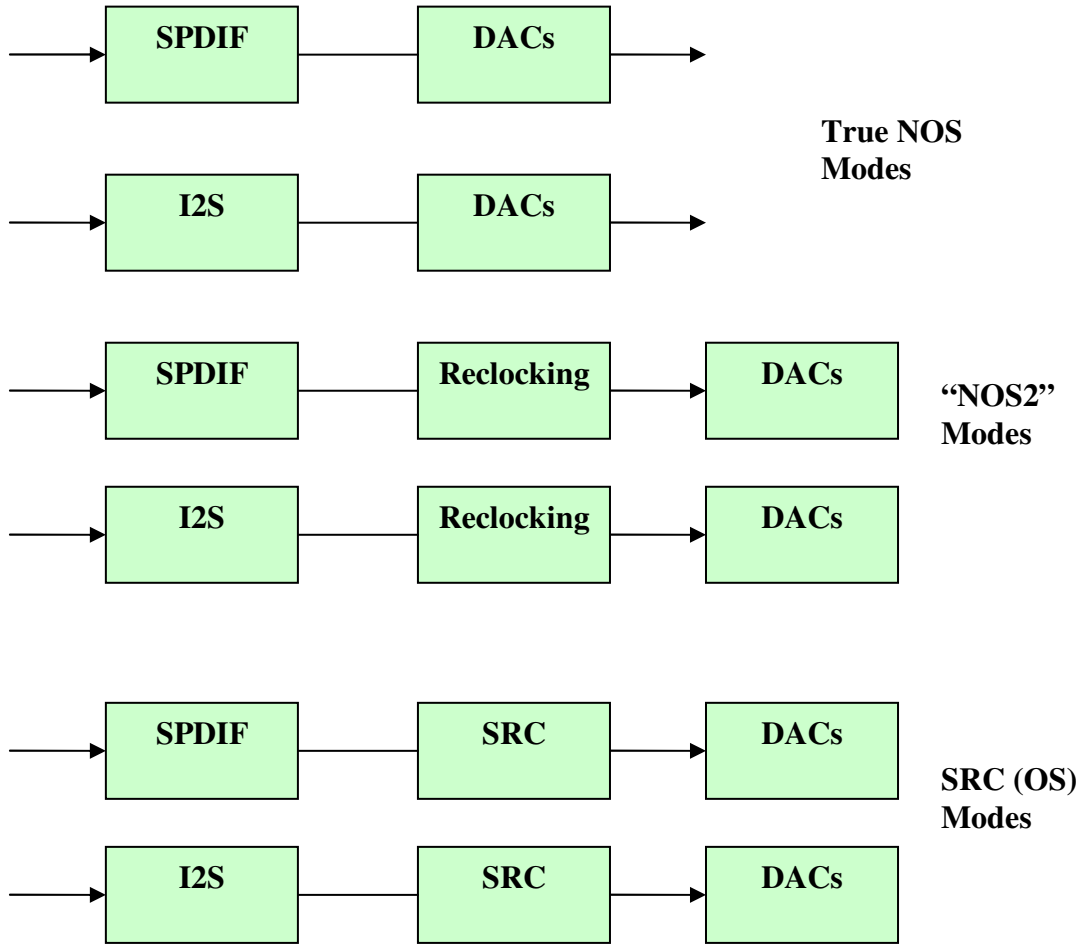
1. Introduction HB-DAC1704-Board Version 3.01 (4/8 DAC Version)

Why again a new DAC design?

There are some reasons for redesigning the old HB_DAC1704 V1.01:

1. Jitter. Again the jitter could be reduced to 0.5..1ps rms in SRC oversampling “mode” (OS).
2. Improved jitter performance in the non-oversampling mode (NOS). The jitter could be decreased to 50ps rms.
3. Extreme improvement in noise with the 4 layer pcb and additional shunt regulator power supply

2. Modes
These modes are switchable:



2.1 NOS Mode

Here can be found an article from Ryohei Kusunoki (http://www.sakurasystems.com/articles/Kusunoki.html) explaining the advantages of the NOS Modes. This is the simplest mode but also the mode where the audio data will not be changed anywhere. The data will we received by SPDIF or I²S and feed directly to the DACs. Only a lossless format conversion occours. The disadvantage is that there could be alaising problems with lower frame rates because it is absolutely difficult to build good analogue filters with a high stop band attenuation for a framerate of e.g., 44.1kHz, with respect to low phase destortion and constant group delay. But this mode could make sense with higher framerates where it is much easier to build e.g. 6dB filters which maybe OK for 172.6kHz or 192kHz.

The jitter depends directly on the quality of the I²S signal or on the quality of the PLL of the SPDIF receiver. With a jitter of 50ps, this PLL is one of the best in the market.

2.2 NOS2 Mode

This mode (also described below) is a NOS mode with re-clocked signals. The DACs input signals are re-clocked by the very low jitter 27MHz Oscillator placed on board.

2.3 SRC (OS) Mode

This mode adds a sample rate converter (SRC) in the chain. This SRC has two functions: First to convert a low sample rate to a constant higher sample rate with the benefit of better analogue filtering and second to reduce the jitter by a foctor of more than 50. A highly stable and low jitter oscillator with its own power supply clocks the output of the SRC and synchonized the DACs. So a very low jitter with better than 1ps (typ. 0.5ps of the oscillator) can be realized. This results in a very clean and clear sound. The disadvantage of this concept is having something like an interpolation filter in the SRC and so there is data manipulation. The SRC is a very high quality one and the downsampling is down without filter (direct down sampling) but the advantage of lowest jitter is often worth more than one filter. Note that all common DAC designs need (or have) digital filtering.

3. Interfaces

3.1 SPDIF Interface

The SPDIF receiver is a low jitter receiver which locks on the incoming frame rate frequencies (44.1 kHz, 88.2 kHz, 172,4kHz or 32kHz, 48 kHz, 96kHz or 192kHz). The incoming data are also transmitted 1:1 for further external processing and is available on the SPDIF connector. With a external Toslink module, a optical SPDIF connection is also possible. The SPDIF input is isolated with a transformator. The termination resistors for input or output are selectable, 75 Ohm (SPDIF) or 110 Ohm (AES/EBU).

3.2 I²S Interface

This interface consists of three signals: Bit clock (BCLK), serial data (SDATA) and left/right clock (LRCLK) or word sync. The TTL inputs are 5 Volt tolerant inputs. The BCLK should be driven with a damping resistor (~33..50 Ohm) at the source and over a high quality coax cable. LRCLK and SDATA signals are not so critical but a good cable termination should be done, too.

3.3 Analogue Out Interface

The user can choose between balanced or parallel current output. With **Data Inversion Jumper** assembled both channels are in balanced mode. Pin 3 of the connectors are inverted (I out -). Without jumper the two DAC chips are working in parallel. Then the user has to connect Pin 1 and Pin 3 together to parallel all DACs for one channel.

The DAC itself is the very best R2R DAC (PCM1704) you can buy. The advantage of a R2R DAC in comparison to the sigma delta DAC is a much better resolution in small signals. And this is the most common case with audio in order to have excellent music quality when the music is more silent and more complex instead of loud where the ears distortion is growing and the effects like sound masking occurs.

Up to four DACs per channel are designed in to reduce noise and THD and improve linearity. They can work in parallel or in balanced mode. The balanced mode gives a better noise immunity (common mode rejection).

There are three versions of the board which only differ in the number of DACs: 2,4 and 8 DACs

The intention of the missing post analogue filtering is that everybody can build up their own I/V converter and analogue filters meeting their own goals of realizing ultimate audio quality. The discussions start with resistor quality and end with capacitors and OPVs. What you really need is a

very good low noise power supply of +/-5V and +/- 250 mA each. It should also have low noise in the lower frequency range (<1kHz). Borbely Audio offers all the missing parts in absolutely high quality. The discrete amplifier designs can handle the very high resolution needed to support the small amplitudes that the DACs have.

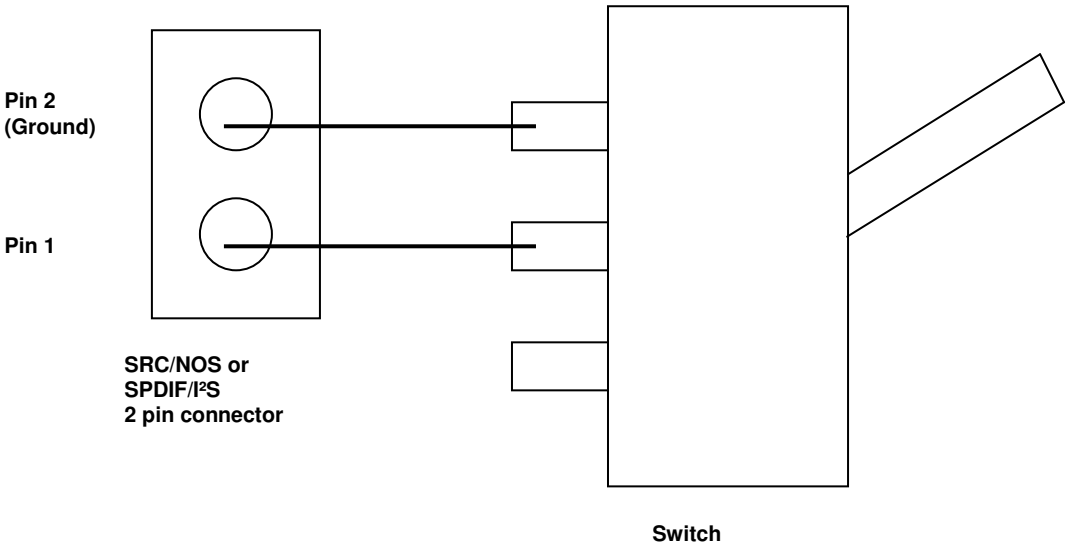
3.4 Power Interface

The board will be delivered with a power connector with coloured cables. **Connect RED to +5V, BLUE to -5V and BLACK to Ground.** The board will be destroyed if you connect it wrong. (It is not possible to plug the connector in the wrong way). Be sure that the voltages are in the specified range (+/-5V, +/-5%). There is no guarantee for incorrectly plugged power connections!

Because the DAC's power supply is also a very important factor regarding the sound quality, we also offer a special shunt power supply including everything except transformer.

3.5 Control Interface

This interface is very simple. You only need two switches for NOS/SRC and SPDIF/I²S. Connect it as follows:



The function select signal has an internal pull up resistor (4.7k Ohm). No connection on the connectors means that I²S input is selected and SRC (OS) is included. It is also possible to drive both signals with other LVTTL logic or microcontroller. Please be aware that these signals are LVTTL level (3.3V tolerant) not TTL (5 Volt tolerant) signals.

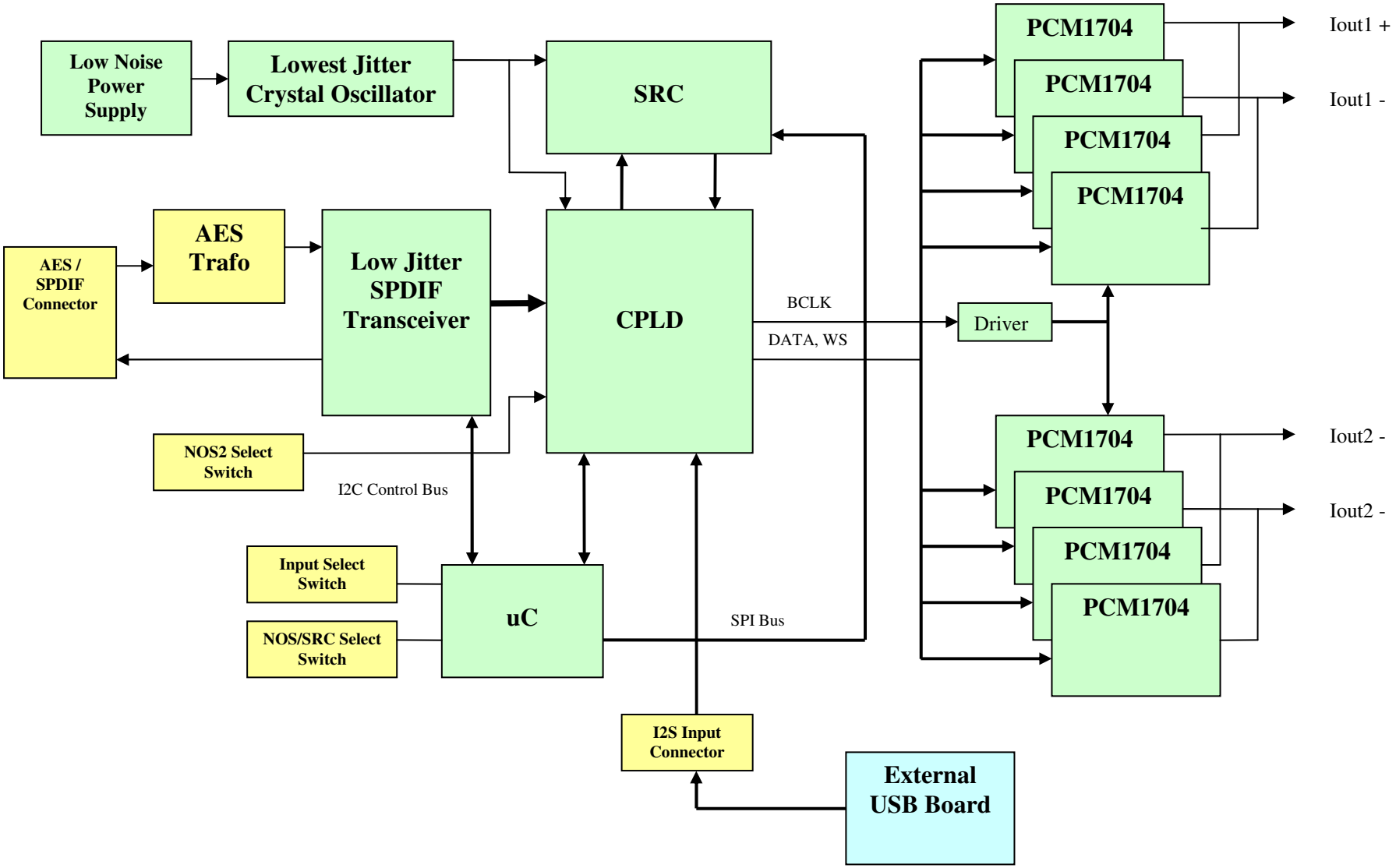
The NOS2 Mode is an added NOS mode done lately in the design process. The connection is a one pin connector which is shorted /switched to ground potential. This can be found at pin 2 of the other switch connectors described above. This mode is chosen if the NOS/SRC switch is switched to SRC.

The function table below explains the different modes.

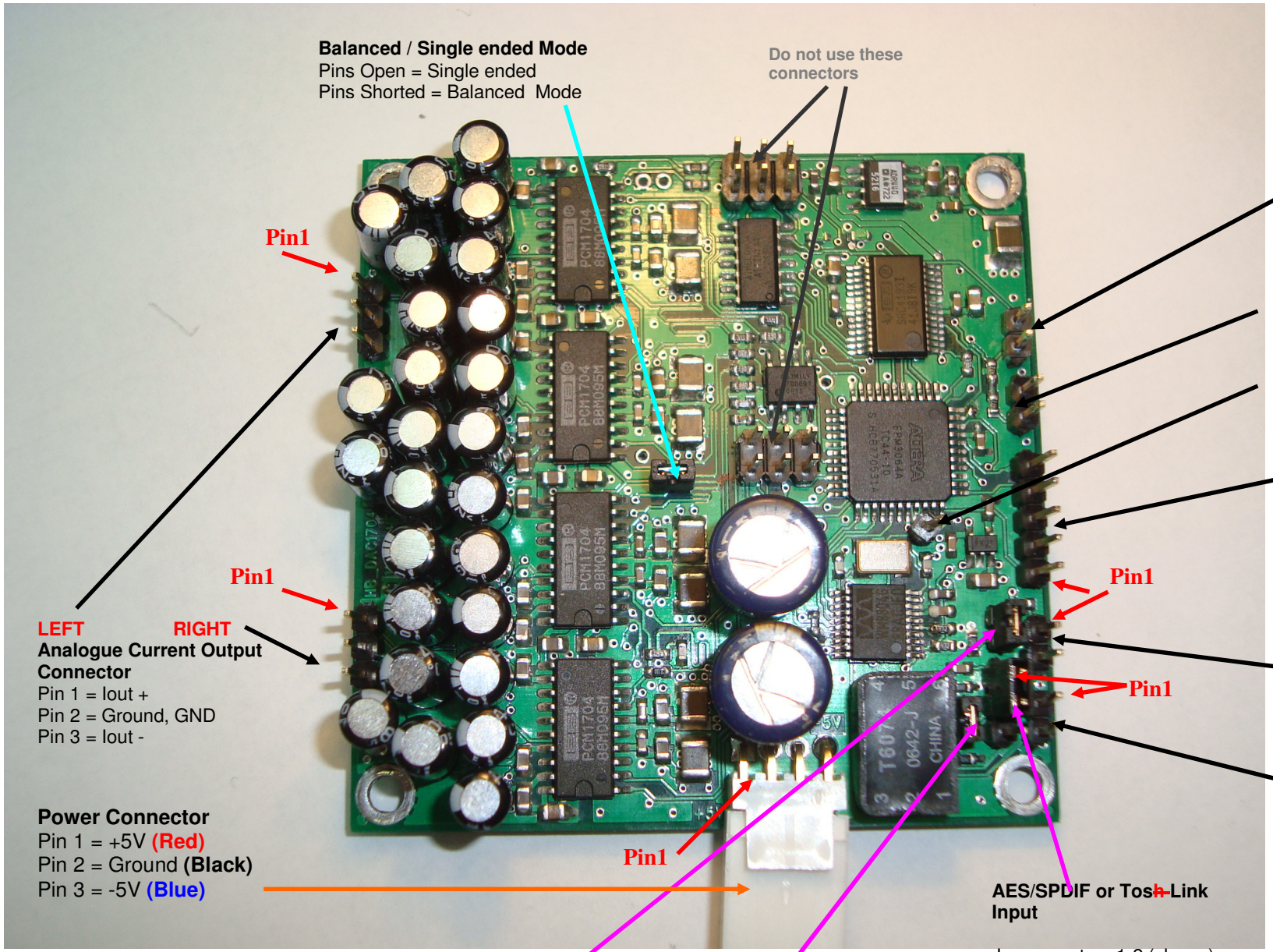
SRC/NOS	NOS2	Functionality
Open	Open	SRC (OS)
Open	LOW (Ground)	NOS2
LOW (Ground)	Open	NOS
LOW (Ground)	LOW (Ground)	NOS

The on board micro-controller (uC) sets all unused chips in total power down for best performance. There is no asynchronous clock from the uC to disturb the signals. The same applies to the other unused parts. So for example when NOS is choosen and I²S input is switched, then the SPDIF receiver, the SRC and the SRC oscillator and the uC in power down. When SRC (OS) and SPDIF is choosen, only the uC is in power down because all other parts are used.

4. Block Diagram



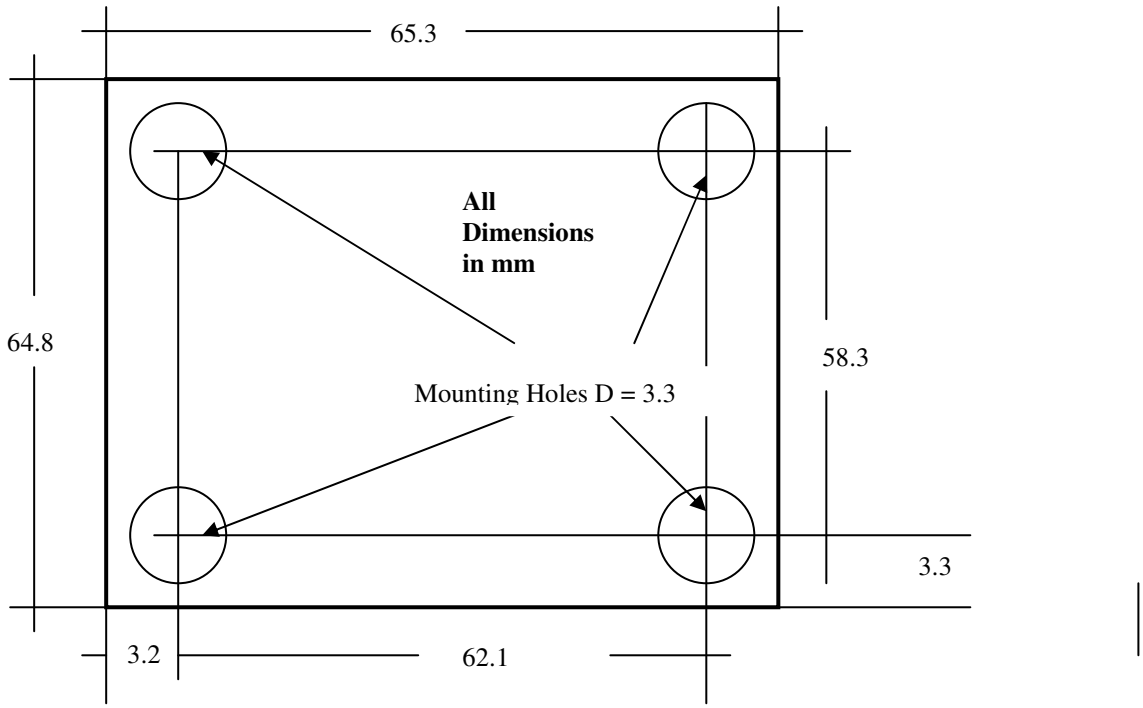
5. How to connect the board



5. Characteristics of HB-DAC1704 Board Version 3.01

- PCB: Version V3.01, 4 Layer,
  Dimensions: 65.3 mm x 64.8 mm
- Supply voltage(s): +/-5V +/-5% regulated, low noise supply required
- Supply current: 200mA for +5V, 230mA for -5V
- Inputs: 1x AES/EBU input, 75/110 Ohm, isolated with signal transformer,
  or 1x Tosh Link data input
  1 x I²S input (header)
- Outputs analogue: Balanced Mode: 4 x Current outputs, max. 2.4 mA/output, Stereo,
  SE Mode Channel with 4 DACs in parallel
  selectable with Jumper
- Control Interface: Tree Switches connectable
- Input Sample Rate: SRC: 4 kHz to 192 kHz
  NOS, NOS2: 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, 192kHz
- DAC Sample Clock: SRC: 210kHz
  NOS: like above
  NOS2: Asynchronously re clocked with 27MHz
- System Clock: 27MHz, Period Jitter of oscillator typ 0.5ps rms
- Micro Controller: always in total power down, except by channel changing or during init
- THD: PCM1704UK: 0.0008%
- Noise: Depends on the noise of the power supply (>=120dB, typ.)

6. Mechanical Dimensions



7. Photos